LAUTERBACH
DEVELOPMENT TOOLS

Intel® Application Note for Server Setup

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MANUAL

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Introduction

This document explains the configuration of TRACE32 for Intel® Xeon® server systems.

Prerequisites

Server debugging requires a debug probe with support for 2 TCK's:

- QuadProbe (LA-4607, LA-4614)

How This Manual is Organized

- **"Server Board Topologies"**: An overview of server board topologies.
- **"Standard Setup"**: Standard setup with auto-detection.
- **"Manual Setup"**: Setup without auto-detection.

Related Documents

- General setup for Intel® x86 debuggers: **"Intel® x86/x64 Debugger"** (debugger_x86.pdf)

Contacting Support

Use the Lauterbach Support Center: https://support.lauterbach.com

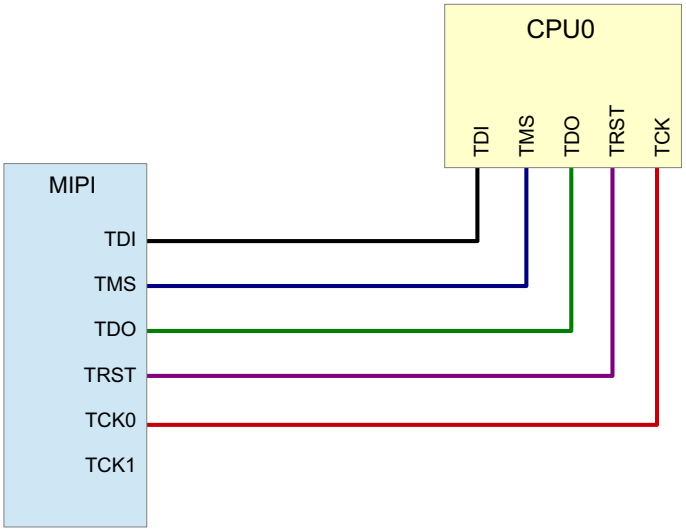
- To contact your local TRACE32 support team directly.
- To register and submit a support ticket to the TRACE32 global center.
- To log in and manage your support tickets.
- To benefit from the TRACE32 knowledgebase (FAQs, technical articles, tutorial videos) and our tips & tricks around debugging.

Or send an email in the traditional way to support@lauterbach.com.

Server Board Topologies

A server board can have 1, 2 or 4 CPU sockets (1S, 2S or 4S system). The board topology is selected with the command **SYStem.Option.TOPOlogy**. The typical board topologies for server systems are:

Figure 1: Single CPU Topology (1S)

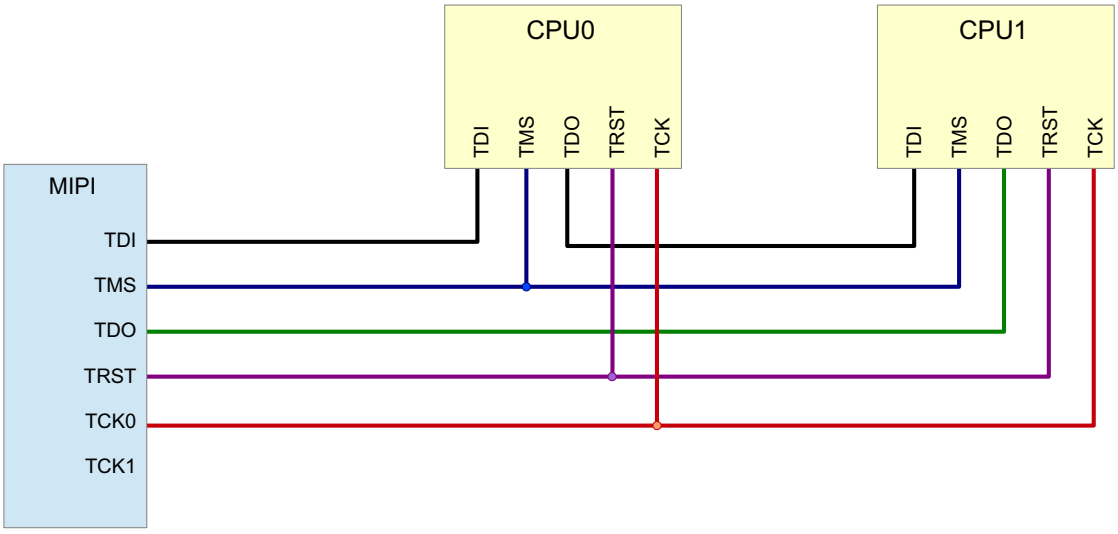


1X1

The 1S server topology (1 chain, 1 socket) is selected with:

```
SYStem.Option.TOPOlogy 1X1
```

Figure 2: Dual CPU Topology (2S)

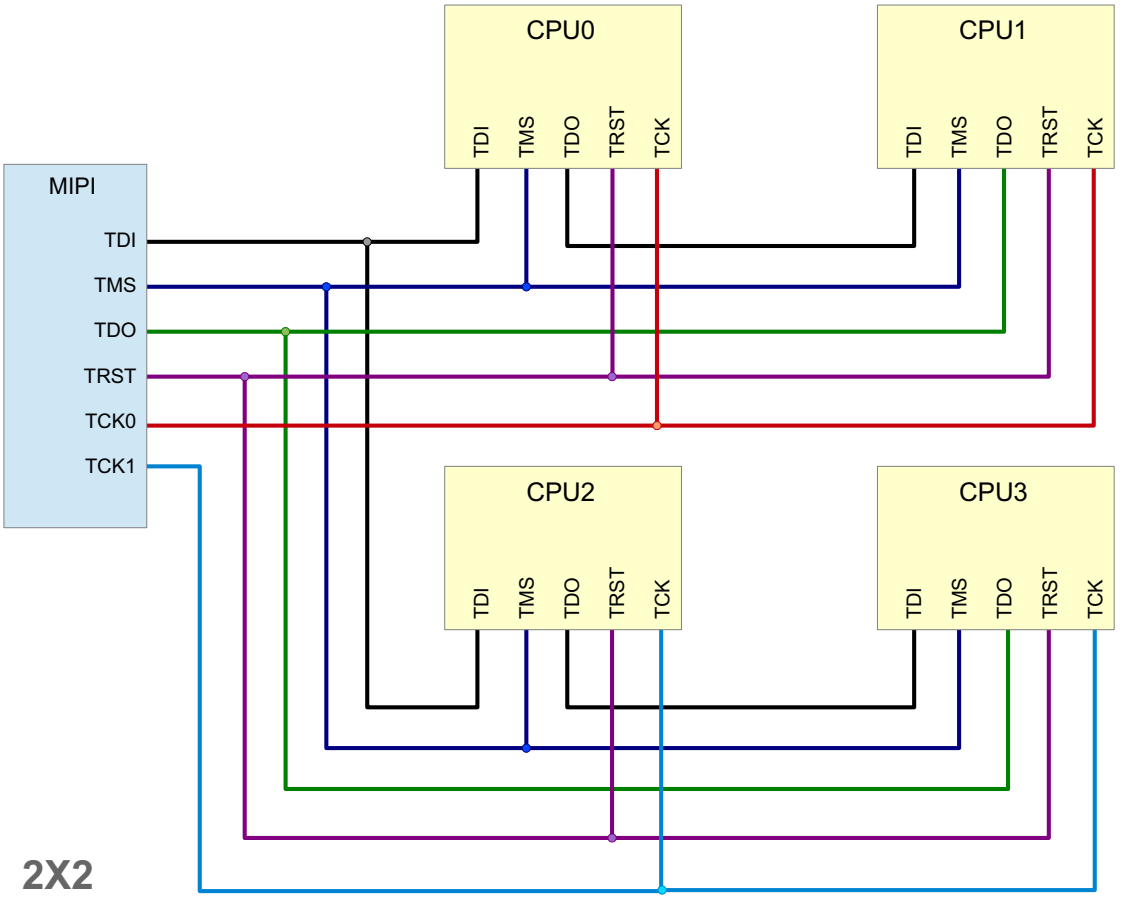


1X2

The 2S server topology (1 chain, 2 sockets) is selected with:

```
SYStem.Option.TOPOlogy 1X2
```

Figure 3: Quad CPU Topology (4S)



The 4S server topology (2 chains, 2 sockets) is selected with:

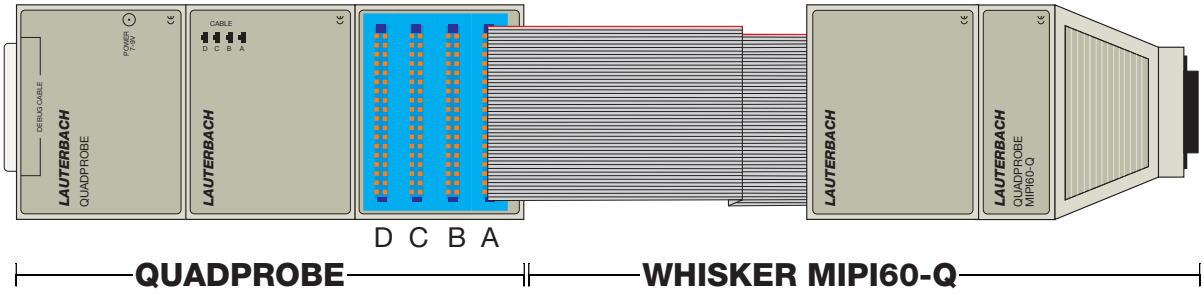
```
SYStem.Option.TOPOlogy 2X2
```

Probe Whiskers

The Quadprobe can control four whiskers, named with A, B, C and D. Each of these whiskers has two JTAG chains:

- A0 and A1 for whisker A
- B0 and B1 for whisker B
- C0 and C1 for whisker C
- D0 and D1 for whisker D

For a debug session it is required to select the needed whiskers with the command **SYStem.Option.MultiCoreWhiskers**. Only the whiskers with the CPU JTAG chains must be selected.



Standard Setup

The standard setup works in most cases. The server board must be powered and the debugger must be connected to the board.

The standard setup consist of the following steps:

1. Configure board topology.
2. Assign the required whisker(s).
3. Detect the CPU.
4. Detect the number of cores/threads.

Standard setup for a 1S system:

```
SYStem.RESet
SYStem.Option.TOPOlogy 1X1
SYStem.Option.MultiCoreWhiskers A0
SYStem.DETECT CPU
SYStem.DETECT CORES

SYStem.Mode Attach
```

Standard setup for a 2S system:

```
SYStem.RESet
SYStem.Option.TOPOlogy 1X2
SYStem.Option.MultiCoreWhiskers A0
SYStem.DETECT CPU
SYStem.DETECT CORES

SYStem.Mode Attach
```

Standard setup for a 4S system:

```
SYStem.RESet
SYStem.Option.TOPOlogy 2X2
SYStem.Option.MultiCoreWhiskers A0 A1
SYStem.DETECT CPU
SYStem.DETECT CORES

SYStem.Mode Attach
```

Manual Setup

In some situations it may be required to set up the debug session manually, e.g. if the session must be configured before the board is powered.

The manual setup consist of the following steps:

1. Configure board topology.
2. Assign the required whisker(s).
3. Select the CPU.
4. Set the hyper thread status.
5. Select the number of threads.

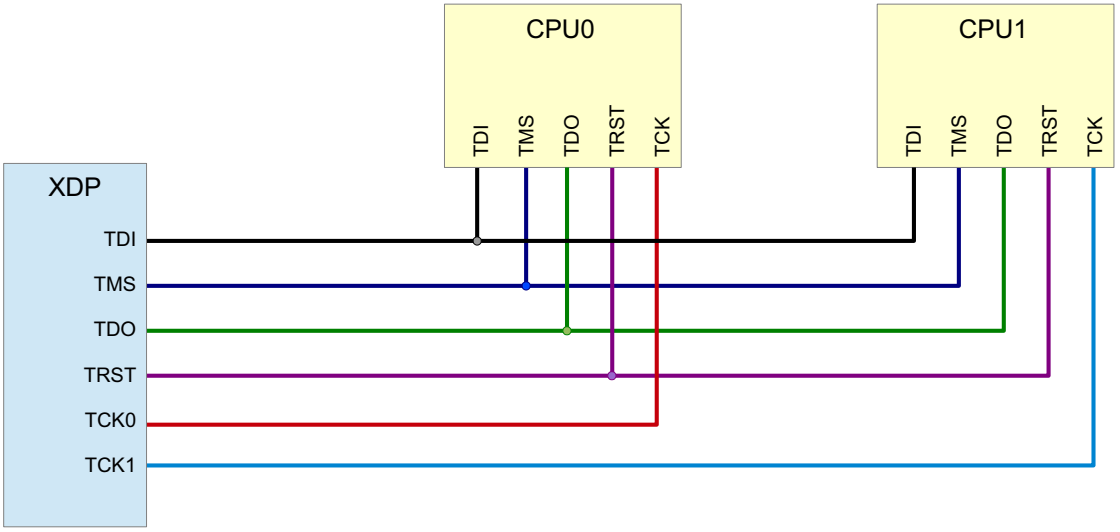
Manual setup for a 2S system (Haswell server, Hyperthreads enabled, 14 cores/CPU-> total 28 cores/56 threads):

```
SYStem.RESet
SYStem.Option.TOPOlogy 1X2
SYStem.Option.MultiCoreWhiskers A0
SYStem.CPU HASWELLSERVER
SYStem.Option.NoHyperThread OFF
CORE.NUMber 56.

SYStem.Mode StandBy
```

If the server board does not use a standard topology as described in section **"Server Board Topologies"**, the first two steps of the setup routine must be adapted:

Figure 4: Dual CPU Topology (2S, two chains)



2X1

This 2S server topology (2 chains, 1 socket) is selected with:

```
SYStem.Option.TOPOlogy 2X1
SYStem.Option.MultiCoreWhiskers A0 A1
```