

Modifying Xilinx ML605 for Direct JTAG Access






Release 09.2024

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Introduction

The ML605 board does not have a JTAG connector but only a USB-JTAG bridge that is connected to the host via a standard USB cable. For debugging with TRACE32, the ML605 needs to be modified in order to make the JTAG signals accessible. This document describes this modification.

The modification was tested and found working by Lauterbach but there is no guarantee whatsoever. In particular be aware that soldering may cause permanent damage to the board.

NOTE:	While the board is modified for JTAG access, the USB-JTAG bridge is disabled. See section “Using ML605 without USB-JTAG bridge” for more information.
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Requirements

The following items are used for accessing the JTAG signals on ML605:

- EVB Xilinx ML605
- Xilinx HW-FMC-105-DEBUG daughter board. The daughter board is not strictly required but serves as a convenient access to the JTAG signals of the main board.
- A Lauterbach “JTAG to Xilinx ML605” adaptor. It may be replaced by a custom-made adaptor. For details, see the section “Pinout of the JTAG to Xilinx ML605 adaptor”.
- Soldering material

Description of the Modification

This section describes the steps to make the JTAG signals accessible for debugging. The description assumes a board orientation with the display towards the user (“South”) and the connectors for the adaptor cards (HMC LCP, HMC HPC) facing away from the user (“North”).

1. The TDO signal (last device) is retrieved by soldering a cable to the left pin of the resistor R296. The cable is later connected to the free pin on the “PPC to HW-FMC-105-DEBUG” adaptor.

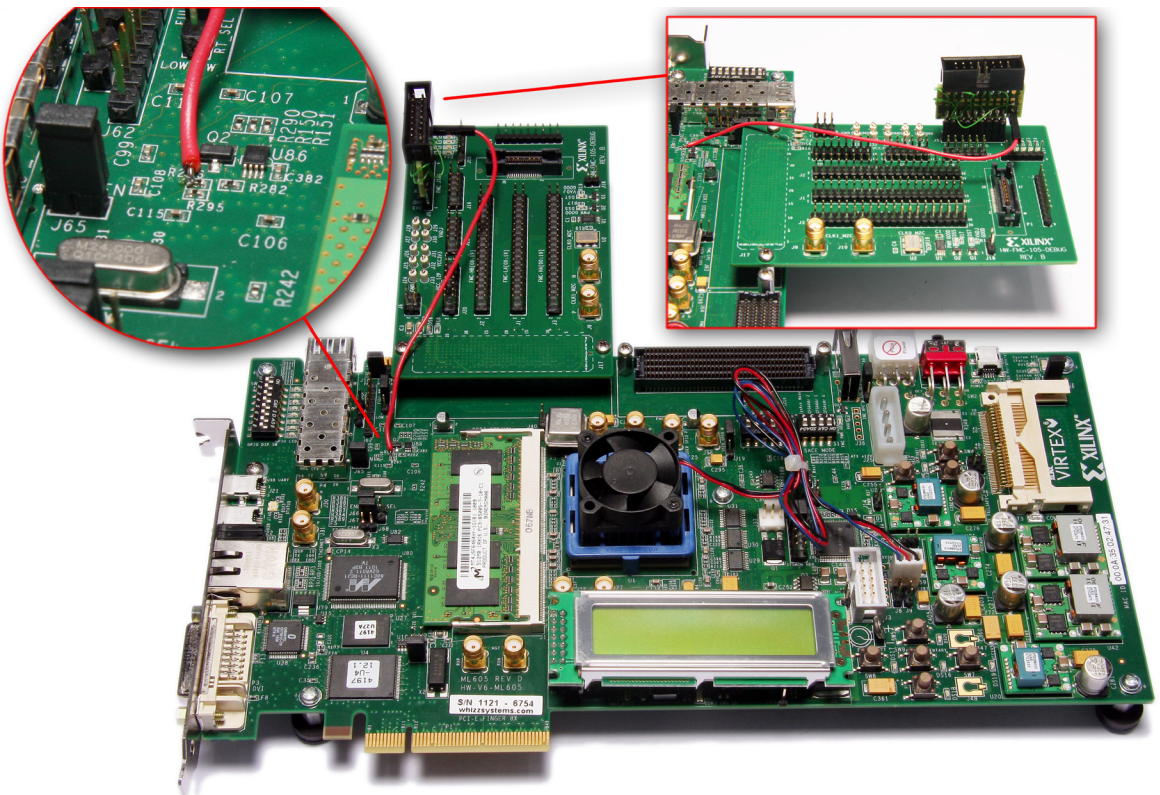
The resistor R296 is located at the front side of the board, close to the south-west corner of the FMC LPC connector.

2. Disable the driver U88 (SN74LV541APWR) so that the debugger can drive the signals. U88 is located at the back side in the north-west quadrant of the board.

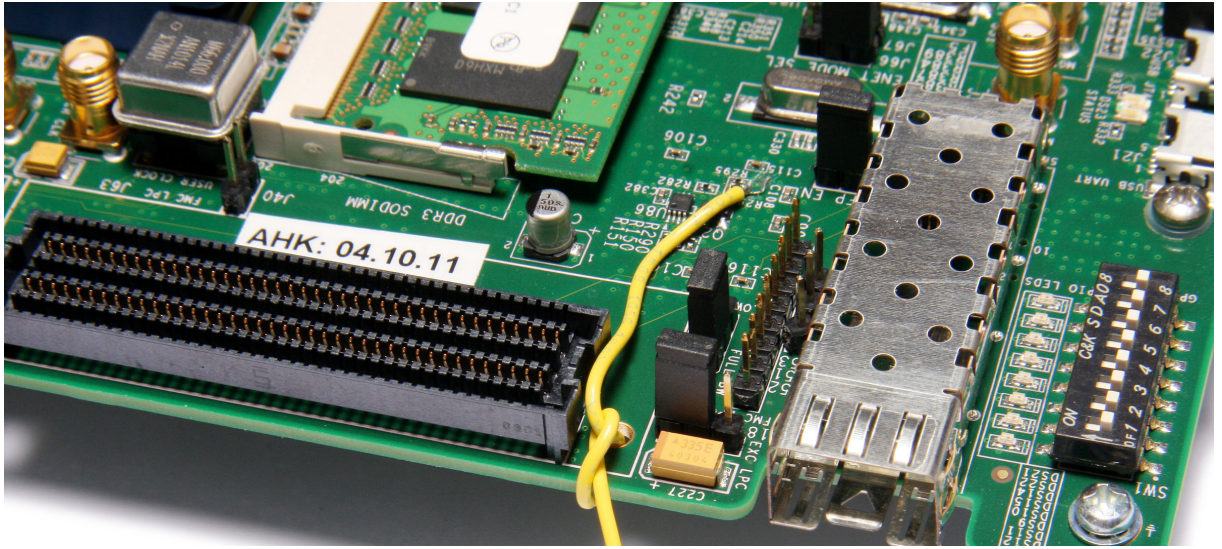
The driver is disabled by bowing up pin 19 (OE2_N) and connecting it to pin 20 (creating a connection to VCC). Also connect pins 16 & 17 and pins 13 & 14 so that the debugger can drive the TMS and TCK nets for the SysACE and Virtex6.

3. Attach the HW-FMC-105-DEBUG daughter board to the FMC-LPC connector J63. Jumper J17 to “EXC HPC” and **J18 to “INC LPC”** settings. Attach the “JTAG to Xilinx ML605” adaptor to J5 on the daughter board. Connect the cable from R296 to the free “needle” on the “JTAG to Xilinx ML605” adaptor.

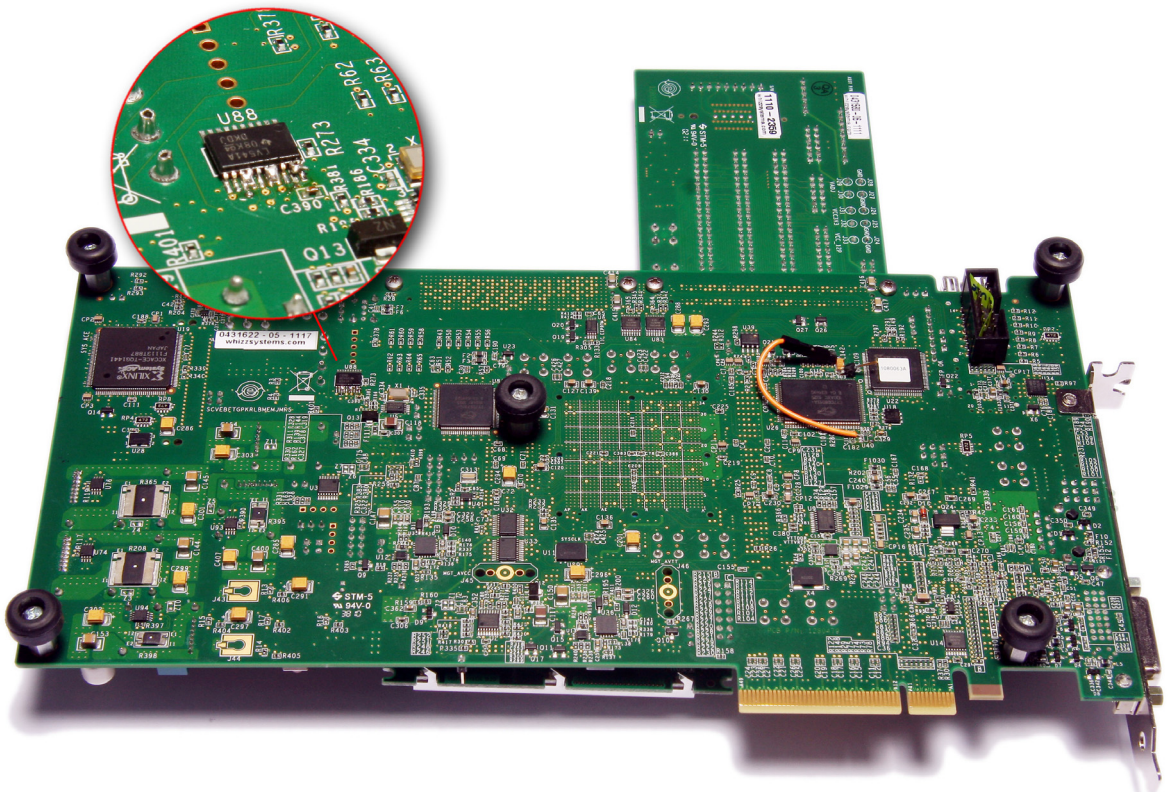
Target top view, cable for TDO attached to R296 (left), JTAG to Xilinx ML605 adaptor (right). In the PDF version, you can zoom into the photo for details.



Accidentally pulling on the TDO cable connected to the resistor R296 can easily tear it off and may be difficult to repair, especially if the pad is also torn off. An improvised cable anchorage with a knot of the cable in a hole besides the FMC LPC connector was found useful for preventing this.



Target bottom view of the board with the disabled driver U88. The orange cable at the right side of the picture is not relevant for our purpose (zoom into the photo for details).



Testing the Modified ML605 Board

For testing the modified board start a TRACE32 for MicroBlaze or PPC and enter the scan chain diagnostic command:

```
SYStem.DETEct.DaisyChain ; scan chain diagnostic
```

The output should be as follows:

```
JTAG Chain Diagnostics
Sum of length of all IR registers      : 18
Number of JTAG devices (BYPASS registers) : 2
IDCODE of device 0 is : 0x0a001093 (Xilinx, XILINX System ACE
controller)
  SYS.CONFIG.DRPOST 0. SYS.CONFIG.DRPRE 1.
  SYS.CONFIG.IRPOST 0. SYS.CONFIG.IRPRE 10. (IRWIDTH 8.)
IDCODE of device 1 is : 0x64250093 (Xilinx, XILINX Virtex-6 XC6VLX240T)
  SYS.CONFIG.DRPOST 1. SYS.CONFIG.DRPRE 0.
  SYS.CONFIG.IRPOST 8. SYS.CONFIG.IRPRE 0. (IRWIDTH 10.)
```

If the debugger reports an error, please check that all steps for the modification were done correctly and in particular a correct setting of the mentioned jumpers.

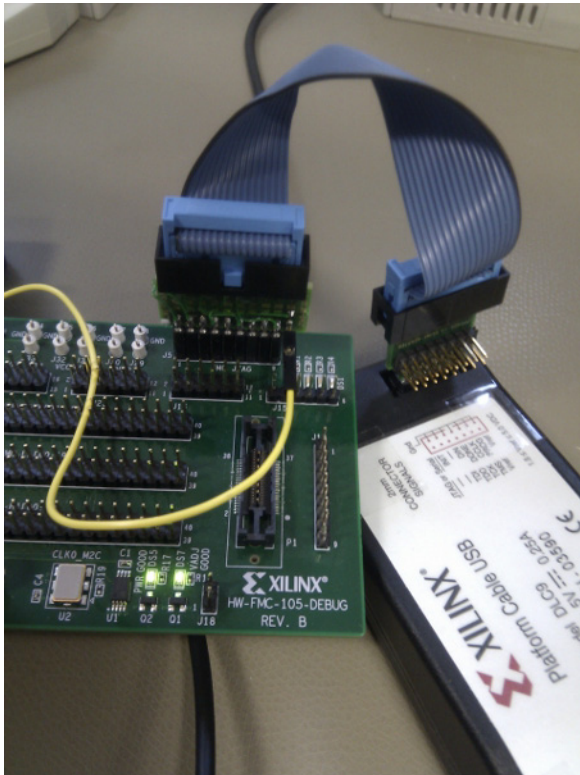
NOTE:	<p>Do not use the given configuration settings for debugging MicroBlaze cores. They do not take into account that only 6 of the 10 bits of the Virtex6's ID register are used for accessing the MicroBlaze core.</p> <p>The correct settings for debugging MicroBlaze are:</p> <pre>SYS.CONFIG.IRPRE 0. SYS.CONFIG.DRPRE 0. SYS.CONFIG.IRPOST 12. ;IRPOST bits: 4 unused + 8 SysACE SYS.CONFIG.DRPOST 1.</pre>
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Using ML605 without USB-JTAG Bridge

While the board is modified for use via a JTAG connector, the USB-JTAG bridge is not functional. This is not a problem for TRACE32 because it uses the JTAG connector.

For using the Xilinx tools (iMPACT, ChipScope, ...) you can either use a Xilinx Platform Cable connecting to JTAG (e.g. Xilinx Platform Cable USB) or alternatively use the TRACE32 debug interface as backend for the Xilinx tools. The latter avoids constantly swapping the cable at the JTAG port when switching between debugging and configuration.

For doing **JTAG accesses with the Xilinx platform cable**, you can use the adaptor “JTAG Converter to Xilinx Target Adapter 14” (LA-3731) which is included with TRACE32 for MicroBlaze, the adaptor “JTAG to Xilinx ML605”, and a 16-wire ribbon cable as shown in the image below.

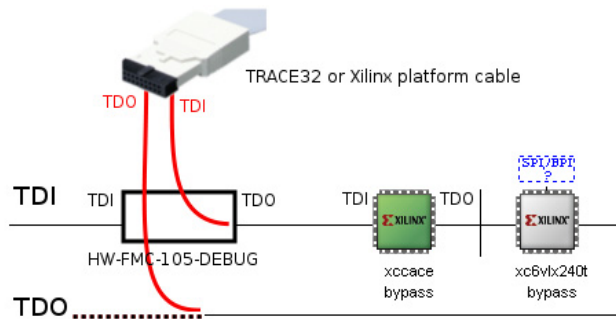


For information on setting up the Xilinx tools for using the TRACE32 debug interface for JTAG access, please refer to the application note “Using TRACE32 as backend for Xilinx tools”.

Pinout of the JTAG to Xilinx ML605 Adaptor

The “JTAG to Xilinx ML605” adaptor converts from the pinout of the Lauterbach TRACE32 PPC dongle (also used for debugging MicroBlaze) to the JTAG header J5 on the HW-FMC-105-DEBUG board.

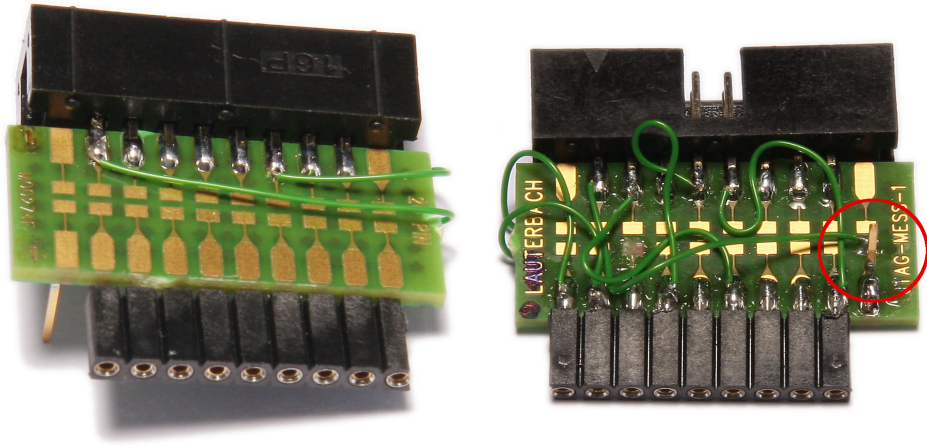
The design needs to take into account that the FMC daughter boards for ML605 are intended to host devices **inside the JTAG chain** i.e. extending the chain by an additional device. The debugger, however, needs to be at the beginning and the end of the JTAG chain to drive the signals. Therefore the adaptor connects its TDI line to the TDO signal of the HW FMC 105 DEBUG board. The additional TDO pin on the adaptor receives the TDO signal of the last device of the board (the Virtex6 FPGA).



PPC dongle			J5 on HW-FMC-105-DEBUG
TDO	1	extra Pin	last device TDO
TDI (TDO_ML605)	3	6	TDO (TDO_ML605)
TCK	7	4	TCK
TMS	9	9	TMS
VCC	6	1	VCC
GND	16	2	GND

NOTE: For trouble shooting or JTAG chain diagnostics you might want to connect a Xilinx platform cable to the HW_FMC_105_DEBUG daughter board. In this case you also need to **cross TDI and TDO** as explained above or connect it to the Lauterbach adaptor.

Photo of the “JTAG to Xilinx ML605” adaptor. The red circle marks the extra pin for the last device TDO.



Miscellaneous Information

This section gives some additional information on miscellaneous topics.

- The schematics of the EVB Xilinx ML605 are available from http://www.xilinx.com/support/documentation/boards_and_kits/xtp052_ml605_schematics.pdf
- The jumper J24 on ML605 cannot be used for JTAG debugging because its JTAG lines are not connected to the SysACE and FPGA. According to a comment in the board schematics it is only intended for reprogramming a CPLD during production testing.