LAUTERBACH
DEVELOPMENT TOOLS

MODULAR, POWERFUL AND FUTURE PROVEN

DEBUG & TRACE SYSTEM
for RISC-V-based SoC

Lauterbach is strategic member of the RISC-V foundation from the beginning. It's leading debug and trace development tools for the embedded industry support all today's chips implementing the RISC-V Instruction Set: Thanks to the long-standing close partnership with RISC-V processor designers and semiconductor manufacturers, future chip developments are also accompanied by Lauterbach from the very beginning – ensuring a future-proof investment.

PowerDebug

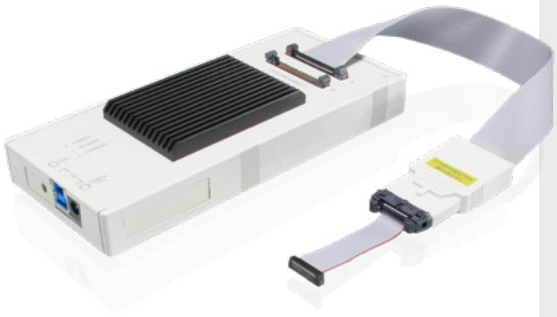
Lauterbach's PowerDebug System is a powerful, modular, flexible debug system that adapts and grows with customers needs when moving from project to project and chip to chip. It can be extended with an optional trace module to debug and trace embedded targets in real-time.

PowerTrace

Lauterbach's PowerTrace extensions provide full insights of what an embedded system is doing without impacting its real-time performance in any way. For system profiling or safety certification trace analysis is essential. In many other use cases it can support in bringing embedded designs to market faster, safer and more reliably than ever.

µTrace Debug-& Trace-Tool

Lauterbach's cost-effective debug solution was developed especially for RV32-RISC-V processors.



KEY-FEATURES:

- Modular system that is designed to grow and adapt as needed. All modules are driven by the same intuitive User Interface to maximize the return on investment.
- Full support of RISC-V debug standard at highest performance.
- Full support of Arm® CoreSight™ and Tessent debug and trace infrastructure.
- Full support of RISC-V CPUs and all common core architectures integrated into your SoC e,g, DSPs, configurable cores such as ARC® and Xtensa®.
- Full support of all RISC-V ISA extensions – standard and custom.
- Advanced debugging features and OS-awareness for popular operating systems like Linux®, Zephyr OS and FreeRTOS™.
- Easy switch from one RISC-V-based SoC to another RISC-V-based SoC while keeping the same debug and trace module and user interface.
- Full remote control and scripting support for test automation and regression tests.
- Full support of future RISC-V Trace standard – Lauterbach is actively working in three RISC-V Processor Trace Task Groups.

NEWS

Simplify Zephyr OS based development in Microchip FPGA SoCs

Lauterbach support the Zephyr® OS when running on SiFive RISC-V CPUs implemented in Microchip's PolarFire® FPGA SoCs (OS awareness).

Full Support for SiFive Automotive Cores

Lauterbach provides full debug and trace support for SiFive automotive CPUs E6-A, X280-A, and S7-A, which address applications like infotainment, cockpit, connectivity, ADAS, and electrification.

Debug Support for Tessent Embedded Analytics Infrastructure

Lauterbach provides support of the features of the Tessent Embedded Analytics IP including RISC-V core trace analysis for single and multicore devices and off-chip trace via Arm CoreSight TPIU or HSSTP using the Tessent ATB interconnect.

Full Trace Support for SiFive Trace Interface

Lauterbach provides full trace support for SiFive Trace Interface implementing Nexus 5001™ trace decoder and parallel off chip trace interface Probe Interface Block (PIB).

Multi-core Vector Processor Debugging of RISC-V AI/ML core

Lauterbach supports all multi-core/multi-cluster configurations of SiFive's 64-bit RISC-V X280 core, as well as all available ISA extensions and Linux debugging.

www.lauterbach.com/risc-v

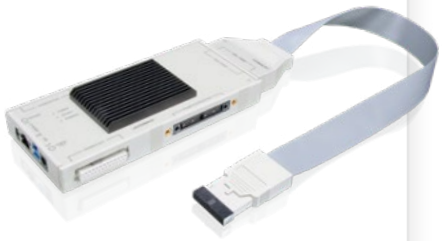
RISC-V

DEBUG- and TRACE-Solutions
for all RISC-V-Cores

µTrace®

Cost-effective
Debug-Tool for
RV32 RISC-V-cores

PowerDebug System

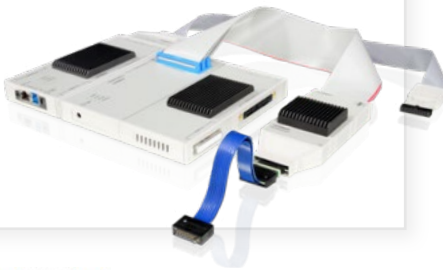


Powerful, modular,
flexible debug system
supporting any
RISC-V-CPU in any chip

DISCOVER MORE:
lauterbach.com/debugger

PowerTrace System

Highest Performance
Trace Recording of entire
RISC-V-based systems



DISCOVER MORE:
lauterbach.com/trace