

TPU Debugger (68332, MPC55x/56x)

- Full support of TPU1, TPU2 and TPU3
- Step and Go commands
- Supports all TPU Breakpoints
- Disassembler for Microinstructions
- Monitor all TPU Registers during stepping
- Modify TPU internal Registers
- Display of Entry Points
- Peripheral View of TPU Registers

The TPU Debugger allows debugging the TPU (Timing Processor Unit) found on many Motorola Devices. It allows setting break conditions on different events and single stepping the TPU microcode while watching the internal registers of the TPU.

Features

TPU Configuration

CH	FUNC	PRIO	HSF	HSR	IEF	ISF	LNK	SGL	CHS	PRM0	PRM1	PRM2	PRM3	PRM4	PRM5	PRM6	P
0	\$9	mid	\$0	\$0	no	yes	no	no	no	009D	A894	0100	0200	AA94	2AE2		
1	\$9	high	\$0	\$0	no	yes	no	no	yes	009D	A993	0200	0100	A993	AA56		
2	\$0	off	\$0	\$0	no	no	no	no	no	0C04	8C0A	6308	1300	5801	0516		
3	\$0	off	low	\$0	no	no	no	no	no	3D00	2900	000C	5146	9000	D000		
4	\$0	off	mid	\$0	no	no	no	no	no	0800	2048	3144	0180	4001	8420		
5	\$0	off	high	\$0	no	no	no	no	no	5000	0010	B090	2A02	8001	301A		
6	\$0	off	\$0	\$0	no	no	no	no	no	200B	22C1	0060	0002	0030	2014		
7	\$0	off	\$0	\$0	no	no	no	no	no	2700	E083	06A8	C108	2001	0012		
8	\$0	off	\$0	\$0	no	no	no	no	no	0498	08C0	020A	9115	6004	8085		
9	\$0	off	\$0	\$0	no	no	no	no	no	0A20	0A43	4081	2202	2001	1044		
10	\$0	off	\$0	\$0	no	no	no	no	no	8900	2B22	0008	1008	2820	1000		
11	\$0	off	\$0	\$0	no	no	no	no	no	829B	0520	0118	4842	1000	4825		
12	\$0	off	\$0	\$0	no	no	no	no	no	600D	4402	0480	8A82	2000	0988		
13	\$0	off	\$0	\$0	no	no	no	no	no	0280	C051	1000	0881	0042	8108		

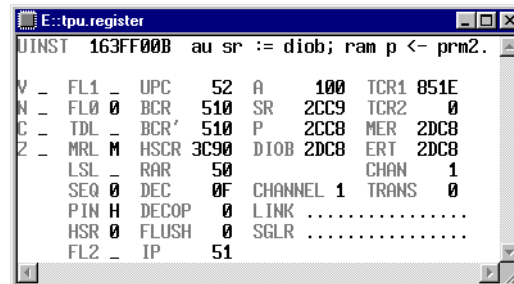
- Peripheral overview of TPU configuration. Can be adapted to support customer specific names for TPU pins and functions.

TPU Program Display

Step	Go	Break	Register
addr	uinst	mnemo	
004F	D451FFFF	call 51; flush.	
0050	525CB5FA	au ert := a + sr; pac := low; neg_mrl; write_mer; cir; end.	
0051	163FF00B	au sr := diob; ram p <- prm2.	
0052	101DF80F	au a := p, ccl; ram diob <- prm3.	
0053	8658FFFF	if LOW_SAME then goto 58.	
0054	36FEB013	au p := diob + sr; ram p -> prm4.	
0055	37FC4FFF	au nil := diob - a, ccl.	
0056	8459FFFF	if LOW_SAME then goto 59.	
0057	D9FF1FFF	return; flush; clr cflg0.	
0058	545CF18A	au ert := sr + diob; pac := no_change; PIN := low; set cflg0; neg_mrl; wr	
0059	545CF14A	au ert := sr + diob; pac := no_change; PIN := high; set cflg0; neg_mrl; wr	
005A	A44EFFFF	if MRL=1 then goto 4E.	
005B	D04FFFFF	goto 4F; flush.	
005C	A45FFEFF	if MRL=0 then goto 5F.	

- Disassembler for the TPU Microcode.

TPU Register Display



```

E::tpu.register
UINST 163FF00B au sr := diob; ram p <- prm2.
V - FL1 - UPC 52 A 100 TCR1 051E
N - FL0 0 BCR 510 SR 2CC9 TCR2 0
C - TDL - BCR' 510 P 2CC8 MER 2DC8
Z - MRL M HSCR 3C90 DIOB 2DC8 ERT 2DC8
LSL - RAR 50 CHAN 1
SEQ 0 DEC 0F CHANNEL 1 TRANS 0
PIN H DECOP 0 LINK .....
HSR 0 FLUSH 0 SGLR .....
FL2 - IP 51
  
```

- TPU Internal Register.

Commands

- Single Step
- Go
- Manual Break
- Breakpoint on Channel
- Breakpoint on uPC
- Breakpoints on special events
- Dump Control Store
- Disassemble Microcode
- Disassemble Entry Points
- Show Peripheral Registers
- Show Internal Registers
- Modify Internal Registers

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