PowerProbe - Logic and Protocol Analyzer

- Timing Analyzer up to 400 MHz
- State Analyzer up to 100 MHz
- 64 Input Channels
- Transient Recording
- Time Correlation with RISC Trace
- Clock Qualifier for State Clock
- Mixed State and Timing Mode
- 4 State Clock Inputs
- Optional FPGA Onchip Trace
- Optional Pattern Generator
- Protocol Support for CAN, USB, etc.

The Timing/State Analyzer Module is special designed for microprocessor applications. It can work separately or in conjunction with all ICD modules. The high-speed transient recording allows very long record time when tracing peripheral lines in a microcontroller application.
Functional Units

Schematics

PowerProbe

Probe Inputs
64 Channels

SOC Connector
32 Channels

Pattern Generator
16 Channels 50 MHz

Pulse Generator
10ns - 40s

Analyzer
64 Channels 100 MHz
32 Channels 200 MHz
16 Channels 400 MHz

Simple Trigger

Trace Memory
64 * 128 (384) K
24 + Timestamp

Complex Trigger
4 Levels, 3 Counters

Asynch Trigger
System Features

- Timing Analyzer with
  - Trace up to 400 MHz
  - Transient recording
  - Simple trigger function
  - Complex trigger function

- Pattern Generator, which can supply 9 channels with a resolution of 20ns

- SOC Connector
- Pulse Generator
- Universal Counter
Trace

Inputs

- 64 Inputs
- 100 KOhm 7 pF 100 Ohm ser.
- 0..+7.0 V
- 1.0 or 1.4 V threshold level separately definable per group
- 4 groups with 16 lines each
- Probe compensation

![Trace Inputs Diagram]

Logical names for input Lines

- Polarity
- Sample Mode
- Groups
- Words

Max. 64 Channels

5 operating modes:
64 channels asynchronous 100 MHz
32 channels asynchronous 200 MHz
16 channels asynchronous 400 MHz

- Up to 32 channels synchronous, 4 clock inputs
- Transient mode

Transient Recording over Required Time
Transient sensitivity can be activated independently for each group. That means, the sampling of the input lines is stored to the trace buffer by the change of the input level only.
The total record time depends on the occurrence of changes on the input signals. The minimum time for high speed signals is 1.2 ms. The max. trace length can be 6.5 h.

Trace Buffer
The depth of the trace buffer is 128K or 256K frames. Each input probe can be used for synchronous or asynchronous events (mixed mode timing/state).
In synchronous mode each recorded frame is marked by a time stamp with a resolution of 10ns.
Display

The contents of the trace buffer can be displayed in a tabular form or as a timing display.
Signal Analysis

- LOAD and SAVE
- COMPARE
- FIND
- Tracking

Master-Slave Operation

- The timing analyzer can trigger the other TRACE32 analyzers (high speed state analyzer or port analyzer)
- The timing analyzer can be triggered by the other TRACE32 analyzers.

Output Formats

- Binary
- ASCII
- VHDL
- Verilog
Option SOC Adapter

Function
The SOC adaption is a simple way of analyzing internal nodes in FPGAs or ASICS. By integration of a scanner module up to 1024 channels can be traced inside a silicon system. The SOC adaption is scalable up to 32 multiplexed signals.

Scanner Module
The scanner module is available in VHDL, Verilog or AHDL.
Connector type is

**SAMTEC FTE-120-xxxx**

### Signals Connector Version A 32 Bit

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## Connector MICTOR

![Connector MICTOR Diagram]

### Signal Connector Version B (MICTOR)

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Complex Trigger System (optional)

Trigger

- Trigger Conditions
  - HIGH, LOW or DONTCARE for each input
  - Range trigger definitions for each group
- 8 Trigger Events
  - 8 global event, no death time
- Trigger Filter

Freely programmable Trigger Sequencer

- 8 Trigger Events
  - 8 global event, no death time
- Trigger Filter

Input variables
- Trigger events from input
- Bus trigger lines A
- Event counter actions/operations
- Acquisition ON/OFF
- Trigger
- Bus trigger lines A
- Counter enable
- Counter restart
- Sequential triggering through 4 levels

- Programmable trigger delay 0 to 100% of records
- Triggering of other system units

Pretrigger Delay
The pretrigger delay prevents from immediate triggering which generates an nearly empty trace storage. The value can be defined between 0 and 100% of the trace storage.

Trigger Delay
The trigger delay can be 0 to 100 s or 0 to 1000% of the trace storage.
Simple Trigger

Function

The simple trigger systems brings the easy trigger function of a scope to the logic analyzer. Trigger conditions can be set by mouse without any keyboard interaction.

Trigger Comparator

Every input can be used as high, low, rising or falling edge. More than one edge can be combined to generate a valid trigger event.

- Trigger Events
  - Don’t care
  - Low
  - High
  - Rising
  - Falling
Direct setting with mouse

Selection Menu

Other Trigger Inputs

- Intertrigger Bus
  - BUS A
- Asynchronous Trigger
- Pattern Generator
Trigger Filters

**Trigger Filter**
The trigger filter can filter out glitches or runts on the lines. The trigger filter can be set from 0 to 2.5 us.

**Trigger Counter**
The trigger count can be defined from 0 to 16 Mio. trigger events.

**Pretrigger Delay**
The pretrigger delay prevents from immediate triggering which generates an nearly empty trace storage. The value can be defined between 0 and 1000% of the trace storage.

**Trigger Delay**
The trigger delay can be 0 to 100 s or 0 to 1000% of the trace storage.
Asynchronous Trigger System

The asynchronous trigger system can be used to trigger on high-speed events, which are not synchronous to the CPU clock or bus cycle. The trigger reacts on events shorter than 3 ns.

- **Data**
  - Combines 8 Inputs to one trigger signal
  - High, Low, Don’t Care for every bit
  - Positive and negative polarity for trigger output

- **Clock**
  - Same as Data, but 2nd comparator

- **SYNC**
  - Combination of Data and Trigger event
  - Positive and negative Clock edge
  - True and false data event

- **LONGER**
  - Pulse width trigger
  - 10ns .. 3 ms
  - Positive and negative pulse

- **SHORTER**
  - Pulse width trigger
  - 10ns .. 3 ms
  - Positive and negative pulse

- **GLITCH+**
  - Glitch trigger on positive pulse
  - 2..10ns detection

- **GLITCH−**
  - Glitch trigger on negative pulse
  - 2..10ns detection

The trigger output can be used to trigger the port analyzer, the emulator or switched to the frequency counter. Events up to 100 MHz can be measured.
GLITCH

- Glitch trigger on positive or negative pulse
- 2–10ns detection

Activity Display

Every port or external line level or pulse activity can be displayed.

Counter System

Every signal can be selected for the universal counter system on the Trace32 FIRE. Event count and pulse width measurement is possible as well as a frequency test on CPU signals. On external inputs up to 100 MHz for input clocks is possible (Frequency only).
## Pulse Generator

### Rate Generator
- 10 ns .. 40s

### Pulse Width
- 10ns .. 40s

### Trigger
- Extern
- Analyzer Trigger
- BUS A
- Pattern Generator

![Trigger Options](image)
The pattern generator can supply the 16 channels on the connector C and D.

A output probe has to be used.

Channels
- 9 output lines on AUX0 .. AUX8
- 20 ns cycle time

Trigger
- Trigger latch mode
  - Stores trigger event
- Trigger Input
  - BUS A
  - External 4 Lines
- Trigger mode
  - High
  - Low
  - Rising
  - Falling
- Retrigger function
  - Wait for trigger
- Restart trigger output to BUS
  - BUS A

Clock
- Clock enable input
- External/internal clock
  - 50 MHz internal
  - 0 ...50 MHz external
  - Rising/falling edge
  - Single step
- Clock qualifier
  - High
  - Low
  - Don't care
Programming

The programming of the pattern generator is done by a text window. Macros can be used for repeating the same sequence several times.

Pattern Definition
- Stand-by
- Set
- Repeat
- ()
- Delay
- Wait
- Restart
- Stop

Pattern Display

The defined pattern sequence can be displayed as a data listing or a timing diagram.
PowerProbe
Order Information

TRACE32 - Technical Information

Order Information

Module Description

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<td>LA-7930 ICD-PP</td>
<td>ICD PowerProbe State-Timing Analyzer 128K&lt;br&gt;ICD State-Timing Analyzer, 64 Channels 100 MHz, 32 Channels 200 MHz, 16 Channel 400 MHz, Transient Recording, 128 KFrames, 48 Bit Time-Stamp, Trigger Filter, Trigger Delay, etc.&lt;br&gt;Requires PODBUS-Interface, No SOC-CON Support</td>
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<tr>
<td>LA-7931 ICD-PP-256K</td>
<td>ICD PowerProbe State-Timing Analyzer 256K&lt;br&gt;ICD State-Timing Analyzer, 64 Channels 100 MHz, 32 Channels 200 MHz, 16 Channels 400 MHz, Transient Recording, 256 KFrames, 48 Bit Time-Stamp, Complex Trigger, 8 Trigger Events, 4 Trigger Levels, 3 Counters (45 bit), Trigger Filter, Trigger Delay, etc., 50 MHz Pattern Generator (9 bit), Requires PODBUS-Interface, Option for SOC Trace</td>
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<tr>
<td>LA-7933 ICD-PP-EXCALIBUR</td>
<td>Adapter EXCALIBUR / SOC-CON&lt;br&gt;Converter EXCALIBUR (200 pin) to SOCCON (MICTOR)</td>
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<td>LA-7649 CONV-MIC38-2.54MM</td>
<td>Converter Mictor38 to 2.54 mm Connector&lt;br&gt;Converter from Mictor 38 to 2.54 mm Connector</td>
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Detailed Order Information

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