

In-Circuit Emulator for the 80186 and 80196

8086	AM186CU
8088	AM186ED
80C186EA	AM186EM
80C186EB	AM186EMLV
80C186EC	AM186ER
80C186XL	AM186ES
80C188EA	AM186ESLV
80C188EB	AM188EM
80C188EC	AM188EMLV
80C188XL	AM188ER
8XC194	AM188ES
8XC196EN	AM188ESLV
8XC196KB	UT80CRH196K
8XC196KC	DS
8XC196KD	V20
8XC198	V30
AM186CC	V40
AM186CH	V50

- Works with Intel, Microsoft, Borland and many other Compilers
- C++ support
- Up to 40 MHz no-waitstate emulation
- Dual ported memory
- FPU support
- Support for all 5V and 3.3V derivatives
- Banking support for 16 banks (186) or 256 banks (196)
- Supports memory split for program and data
- CASE tools interface
- RTOS support
- Windows9x, NT and X windows interface

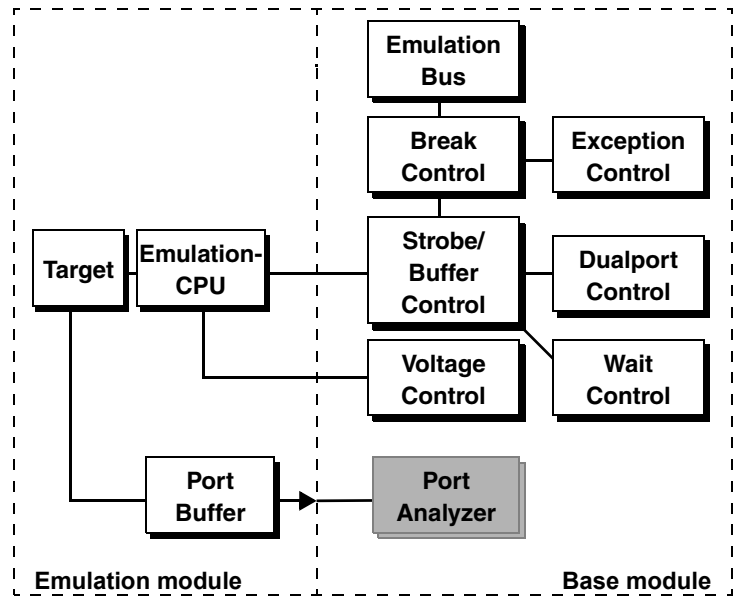
The TRACE32-ICE186 supports microcontroller from AMD, NEC and Intel. Its modular and open technology allows the fast integration of new chip designs.

A software compatible ROM Monitor is also available.

TRACE32 works with the highest variety of host interfaces. The communication link to the host is done by the printer port, a fibre optic interface or ethernet allowing a high-speed transfer.

Features

Basics of Operation



The ICE-186 is a high-performance emulation system. The change between the different supported CPU types is done by changing the emulation module.

On the emulation base there is an extra slot for the TRACE32 Port Analyzer. Depending on CPU type various signals can be traced.

Some probes also have connectors to trace external target lines.

Operating Modes

The emulator can work in stand-alone mode with internal clock or in active mode with internal or the target clock. On power-down of the target system the emulator tristates its output buffers and isolates its internal emulation circuits.

The operation modes are as follows:

- Reset Down
- Reset Up
- Alone Internal
- Alone External
- Emulation Internal
- Emulation External

Clock

- Operation with external or internal clock
- 1..40 MHz internal clock

Bank Support

External bank switching schemes or the MMU can be supported by the memory mapper. Therefore a separate input probe is needed for the emulator.

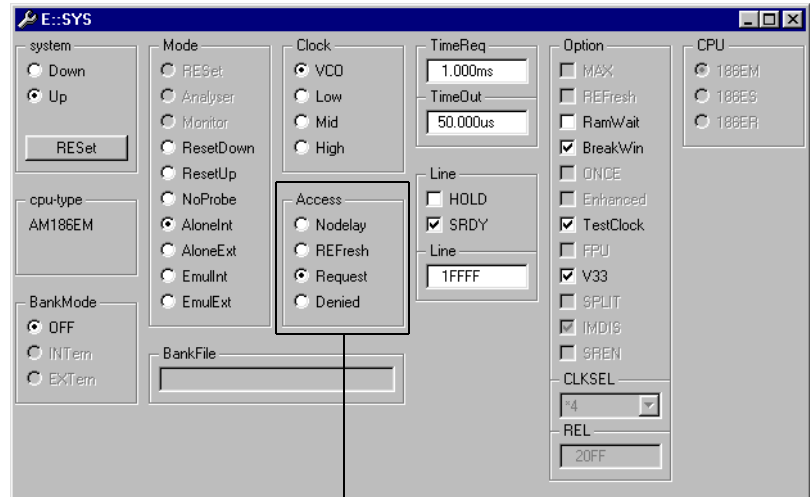
- 16 banks for 186
- 256 banks for 196

Selective Mapping of Memory Classes

The address mapper can segment the memory into program and data area. By using this segmentation e.g. it is possible to map the program area to

the emulation memory while the RAM area remains mapped to the target memory.

Dual-Port Access



Dual port access modes

All TRACE32 memories are dual-ported. The dual-port access makes it possible to display and modify the contents of the overlay memory, to set or delete breakpoints or use the flag memory while the application is running in real-time.

The following dual-port access modes are implemented:

- Nodelay
- REFresh (not 196)
- Request (not 196)

In the **Nodelay mode** the dual-port cycle is inserted between the bus cycles generated by the CPU. This means that the max. speed of operation is not possible in this mode, or extra wait states are needed for correct operation.

In the **REFresh mode** refresh cycles of 188/186 Enhanced Mode controller are used to generate dual-port cycles.

In the **Request mode** Hold/HLDA line of the CPU is used to implement dual-port cycles.

In the **Denied Mode** the dual-port access is switched off.

HLL Debugging

The screenshot shows the TRACE32 debugger window with the following assembly code and a context menu:

Step	Step Over	Go Next	Go Return	Go Up	Go	Break	Mode
addr/line	code	label	mnemonic	comment			
				register int i, prime, k; int count;			
568				count = 0;			
P:0040:077F	C746FC0000		mov	word ptr [bp-4],0			
570				for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;			
P:0040:0784	2BF6		sub	si,si			
P:0040:0786	EB08		jmp	790			
P:0040:0788	BBDE		mov	bx,si			
P:0040:078A	46		inc	si			
P:0040:078B	C687D		mov	byte ptr [bx+4D8],1			
P:0040:0790	B3FE1		cmp	si,+12			
P:0040:0793	7EF3		jle	788			
572				i <= SIZE ; i++)			
P:0040:0795	2BF6		sub	si,si			
P:0040:0797	EB26		jmp	7BF			
574				lags[i])			

The context menu is open over the instruction at address P:0040:0784, showing options: Go Till Here, Default Breakpoints, Spotpoint, Set PC Here, Display Memory..., Breakpoints..., Go Till..., Edit Source, List There, Assemble here..., and Modify here...

The TRACE32 Debugger supports all standard compilers for C and C++. For more information refer to the section "Debug Interfaces".

Full support in real-time for:

- Break-before-line operation
- HLL single step in real-time
- Trigger and trace on local variables

Background Task

The background task allows:

- To process interrupts

- To maintain the refresh of a target DRAM

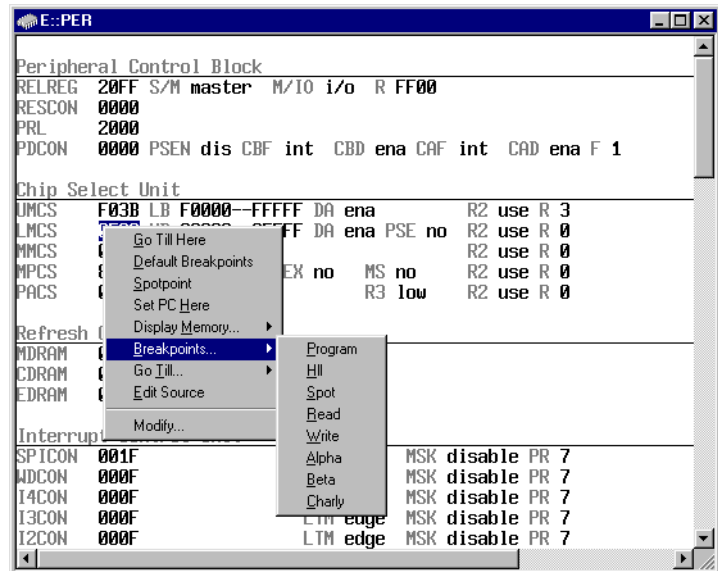
while the emulation is stopped.

Wait System

- Additional wait cycles (1-15) may be specified

- Up to 250 wait cycles (4K blocks global and bitwise)

CPU Peripherals



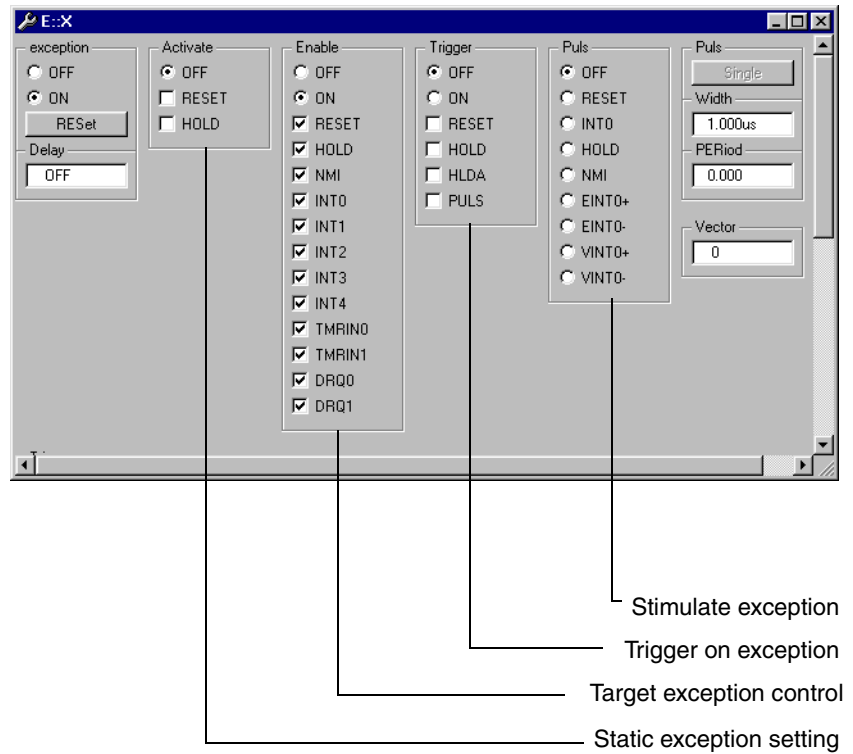
- Display of onchip peripherals
- Pull down menus for settings
- User definable display of the onchip peripherals
- Additional description for each field
- Definition is done interactive supported by softkeys
-

FPU Support

Register	Value	Address
IM I IE _ C0 _ CW	03FF	ST(0) 3.1415926
DM D DE _ C1 _ SW	3C00	ST(1) NAN
ZM Z ZE _ C2 2 TW	3FFF	ST(2) NAN
OM O OE _ C3 _ TOP	7	ST(3) NAN
UM U UE _ B _		ST(4) NAN
PM P PE _ OPC	04C0	ST(5) NAN
PC E SF _ IP	00000005	ST(6) NAN
RC N ES _ OP	00000100	ST(7) NAN

The display and modification of the FPU registers is supported.

Exception Control



The TRACE32 exception controller allows to permanently activate an exception, to enable or disable specific

exceptions, to trigger on specific exceptions or to stimulate an exception.

Clock Fail Detection

On-Circuit Emulation

- Supports the ONCE mode Clip-Over adaptation

Modules Overview

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Debug Interfaces

TRACE32-PowerView supports most compilers, realtime operation systems and debuggers.

New integrations are mostly done on customers request. If your compiler or RTOS is not supported now, please ask us !

Compiler Support 186

CPU	Language	Compier	Compan y	Option
X86 REAL	ASM	AXLS		HP
X86 REAL	C	BORLANDC	Borland Software Corporation	EOMF-86
X86 REAL	C	ORGANON	CAD-UL Electronic Services GmbH	EOMF-86
X86 REAL	C	IC86	Intel Corporation	OMF-86
X86 REAL	C	MCC86	Mentor Graphics Corporation	EOMF-86
X86 REAL	C	MSC/MSVC-16BIT	Microsoft Corporation	EOMF-86
X86 REAL	C	MSC/MSVC	Microsoft Corporation	EXE/TD
X86 REAL	C	ICC86	TASKING	OMF-86
X86 REAL	C	ICC86	TASKING	IEEE

CPU	Language	Compiler	Company	Option
X86 REAL	C++	BORLANDC	Borland Software Corporation	EXE/TD
X86 REAL	C++	MSVC-16BIT	Microsoft Corporation	EXE/CV
X86 REAL	MODULA	LOGITECH-M2	Terra Datentechnik	MAP/REF
X86 REAL	PASCAL	TEK-PASCAL	Tektronix	TEK
X86 REAL	PLM	PL/M86	Intel Corporation	OMF-86

Compiler Support 196

CPU	Language	Compier	Compan y	Option
80196	C	ICC196	IAR Systems AB	UBROF
80196	C	IC96	Intel Corporation	OMF-96
80196	C	C196	TASKING	OMF-96
80196	PLM	PL/M96	Intel Corporation	OMF-96

RTOS Support

Debugger Support

CPU	Debugger	Company
	WINDOWS CE PLATF. BUILDER	-
	CODE::BLOCKS	-
	C++TEST	-
	ADENEO	-
	X-TOOLS / X32	blue river software GmbH
	CODEWRIGHT	Borland Software Corporation
	CODE CONFIDENCE TOOLS	Code Confidence Ltd
	CODE CONFIDENCE TOOLS	Code Confidence Ltd

CPU	Debugger	Company
	EASYCODE	EASYCODE GmbH
	ECLIPSE	Eclipse Foundation, Inc
	CHRONVIEW	Inchron GmbH
	LDRA TOOL SUITE	LDRA Technology, Inc.
	UML DEBUGGER	LieberLieber Software GmbH
	SIMULINK	The MathWorks Inc.
	ATTOL TOOLS	MicroMax Inc.
	VISUAL BASIC INTERFACE	Microsoft Corporation
	LABVIEW	NATIONAL INSTRUMENTS Corporation
	RAPITIME	Rapita Systems Ltd.
	RHAPSODY IN MICROC	IBM Corp.
	RHAPSODY IN C++	IBM Corp.
	DA-C	RistanCASE
	TRACEANALYZER	Symtavision GmbH
	TA INSPECTOR	Timing Architects GmbH
	UNDODB	Undo Software
	VECTORCAST UNIT TESTING	Vector Software
	VECTORCAST CODE COVERAGE	Vector Software

Operation Voltage and Frequency

The maximum operation frequency of TRACE32-ICE depends on:

- The max. frequency of the CPU
- The access time of the overlay memory (15ns or 35ns)
- The mapper mode (**S**low or **F**ast)
- The number of waitstates (W0 = 0 waitstates
W1 = 1 waitstate)
- The dual-port access mode

Denied Access

Nodelay Access

Operating Voltage

This list contains information on probes available for other voltage ranges.

Probes not noted here supply an operation voltage range from 4.5V to 5.5V. tbd

Dimensions

Module Dimensions

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Connectors

On each emulation module there are half-size connectors to:

- ❑ Connect the emulation module directly to the target by providing the corresponding connectors also on the target hardware

- ❑ Connect a standard adapter from Emulation Technology, YAMAICHI, AMP, TOKYO ELETECH etc.

The following table lists the physical dimensions of these connectors.

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Adapter

The adapters connect in different ways

- With Clip-Over Adapters the CPU can stay on the target board.
- With Solder-ON adapters the CPU must be removed

- YAMAICHI and AMP adapters fit to the CPU socket

The following table lists the physical dimensions of these adapters.

Not necessary.

Available Tool Chain

TRACE32 provides a complete set of development tools for this family. This includes:

- The In-Circuit Emulator TRACE32-ICE
- The high speed RISC Emulator TRACE32-FIRE
- The BDM/JTAG/ONCE etc. based In-Circuit Debugger TRACE32-ICD
- The ROM Monitor based In-Circuit Debugger TRACE32-ICD
- The ICD Trace, a trace extension to the BDM/JTAG debuggers or ROM monitors
- Evaluation boards, which can be used until the target hardware is available.
- The Instruction Set Simulator (SIM), a software tool for code test without any hardware

The following list give an overview which development tools are available for the specific derivatives of this family.

tbd

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Module Description

Detailed Order Information

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