LAUTERBACH
DEVELOPMENT TOOLS

MODULAR, POWERFUL AND FUTURE PROVEN

Debugger & Trace Solutions for RISC-V®-Based SoCs

Lauterbach has been a strategic member of the RISC-V Foundation from the very beginning. That's why it's leading debug and trace tools have long supported CPU cores implementing the RISC-V instruction set and custom ISA extensions.

With Lauterbach's TRACE32® tools, developers can now debug and control RISC-V cores in almost any combination with other CPU architectures via a single debug interface. In addition, the TRACE32® tools support real-time on- and off-chip tracing for all major RISC-V trace infrastructures.

Thanks to the longstanding close partnership with RISC-V processor designers and semiconductor manufacturers, future chip developments are also accompanied by Lauterbach from the very beginning – ensuring a futureproof investment.

DOWNLOAD OUR SOLUTIONS OVERVIEW

All information about Lauterbach's products for debugging and tracing.

KEY FEATURES

Support for All RISC-V Debug & Trace Interfaces

Lauterbach tools support not only the RISC-V debug standard at highest performance, but also the Arm® CoreSight™ and Tessent debug and trace infrastructure as well as the newest RISC-V trace standards E- and N-trace. Lauterbach is actively working in three RISC-V Processor Trace Task Groups.

Unlimited RISC-V & Multicore Debugging

Many SoCs implement different kinds of cores – besides RISC-V you often find Arm CPUs or other proprietary cores, e.g. DSPs such as ARC® and Xtensa®. No matter what kind of multicore system is used, TRACE32® supports them all.

OS-Aware Debugging of Any RISC-V and other Core

Lauterbach's TRACE32® OS-aware debugging provides key insights into applications and the operating systems they are running on, no matter if rich operating systems like Linux, real-time operating systems (RTOS) such as Zephyr OS and FreeRTOS or a mixture of all is used. With this, engineers can better understand how they are behaving and utilizing chip resources.

One Solution for All of Your Different RISC-V Chips

The modular system that is designed to grow and adapt as needed – from virtual targets and simulators to real silicon. All modules are driven by the same intuitive user interface to maximize the return on investment. Developers can easy switch from one RISC-V-based SoC to another RISC-V-based SoC while keeping the same debug and trace module and user interface.

LEARN MORE @
lauterbach.com

RISC-V

DEBUGGER and TRACE-Solutions
for All RISC-V based SoCs

SUPPORTED SYSTEMS	AVAILABLE TRACE32® SOLUTIONS			
	Debug	On-Chip Trace	Off-Chip Trace	Instruction Set Simulator
RISC-V 32bit RV32	✓ 1 / 2	✓ 1 / 2	✓ 3** / 2**	✓ 4
RISC-V 64bit RV64	✓ 1	✓ 1	✓ 3**	✓ 4
AndesCore™ V5	✓ 1 / 2*	✓ 1 / 2*	✓ 3** / 2* / 2**	✓ 4
SiFive® Core IP	✓ 1 / 2*	✓ 1 / 2*	✓ 3** / 2* / 2**	✓ 4
Synopsys ARC-V IP™	✓ 1 / 2*	✓ 1 / 2*	✓ 3** / 2* / 2**	✓ 4

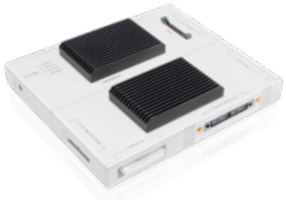
PowerDebug System

1 Powerful, moduler, flexible debug system for 150+ microprocessor families

µTrace®

2 Cost-effective all-in-one debug and trace module

PowerTrace System



3 Highest performance parallel and serial trace system

Instruction Set Simulator

4 ISS for developing or testing application code without target hardware

LEARN MORE ABOUT OUR RISC-V SOLUTIONS

All information about Lauterbach's products for debugging and tracing RISC-V Cores: lauterbach.com/risc-v

* Only 32-bit RISC-V SoCs

** If chip has implemented a dedicated trace-interface