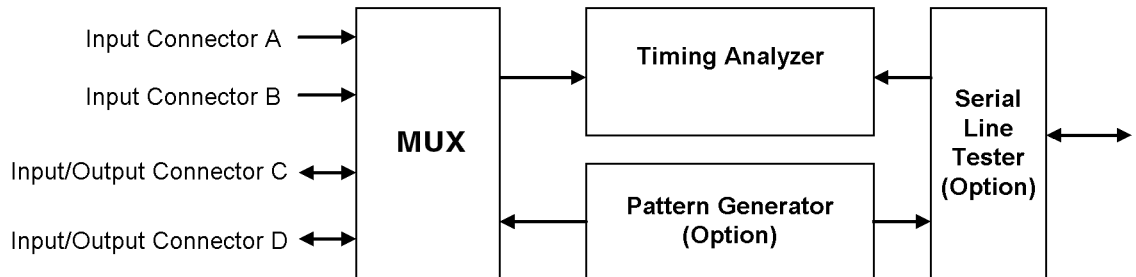


## Timing and Protocol Analyzer

- Timing analyzer up to 200 MHz
- Time correlation with state analyzer
- Selective trace controlled by state analyzer
- State analyzer mode
- 16 channel pattern generator
- 2 channel serial line tester

The Timing- and Protocol Analyzer Module TA32 is special designed for microprocessor applications. It can work separately or in conjunction with the state analyzer module HA120. The high-speed transient recording allows very long record time when tracing peripheral lines in a microcontroller application.

## Functional Units



- Timing Analyzer with
  - Trace up to 200 MHz
  - Transient recording
  - Complex trigger function
- Pattern Generator, which can supply 16 channels with a resolution of 100ns

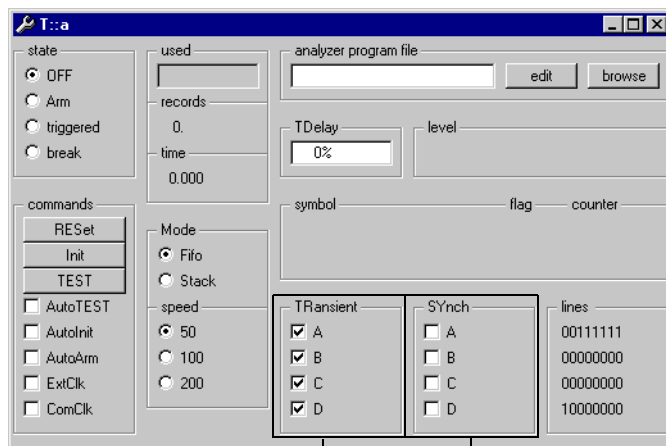
- Serial Line Tester, which can be connected directly to a 25-pin line

For the input and output connectors a separate input or output probe is needed.

## Timing Analyzer

### Logical names for Input Lines

### Max. 32 Channels



Synchronous mode  
for each input connector

Transient mode  
for each input connector

5 operating modes:

- 32 channels asynchronous  
50 MHz (Channel A, B, C, D)
- 16 channels asynchronous  
100 MHz (Channel A, B)
- 8 channels asynchronous  
200 MHz (Channel A)
- 31 channels synchronous  
15 MHz
- Transient mode

### Transient Recording over Required Time

Transient sensitivity can be activated independently for each group. That means, the sampling of the input lines is stored to the trace buffer by the change of the input level only.

The total record time depends on the occurrence of changes on the input signals. The minimum time for high speed signals is 0.6 ms.

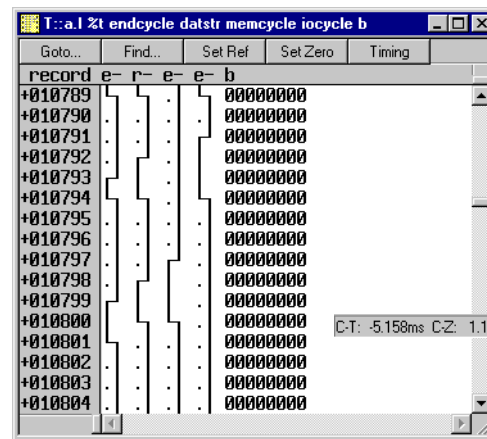
## Trace

The depth of the trace buffer is 32K frames.

Each input probe can be used for synchronous or asynchronous events (mixed mode timing/state).

In synchronous mode each recorded frame is marked by a time stamp with a resolution of 20ns.

## Display

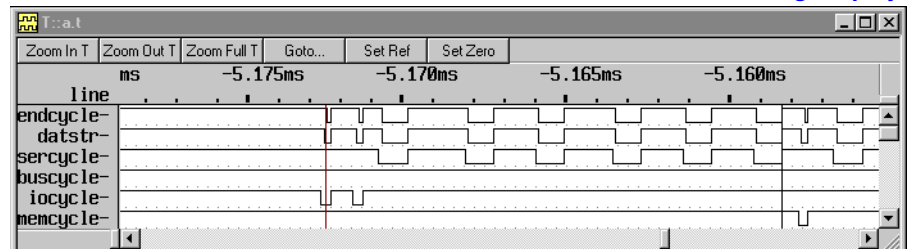


State Display

Cursor Info

C-T: -5.158ms C-Z: 1.154ks C-R: 14.240us -5.179ms -- -5.155ms 0.040us / dot

Timing Display



The contents of the trace buffer can be displayed in a tabular for or as a timing diagram.

## Master-Slave Operation

- The timing analyzer can trigger the other TRACE32 analyzers (high speed state analyzer or port analyzer)
- The timing analyzer can be triggered by the other TRACE32 analyzers.

## Trigger System

- Trigger Conditions
  - HIGH, LOW or DONTCARE for each input
- Range trigger definitions for each group

- 4 Trigger Events
  - 4 global event, no death time
  - 4 events on every trigger level with 20ns death time
- Trigger Filter

### Freely programmable Trigger Sequencer

```

T::a.p
Save Save As... Save+Close Quit+Close Save+Comp Compile
DATA chipselect_1 a:@11111110! b:34
DATA chipselect_2 datstr b:34
EVENT delay 1000.

COUNT delay if datstr:a:chipselect_1
GOTO trigg if delay

trigg:
BREAK if chipselect_2

GOTO CONTInue Sample. OUT. Count. other previous

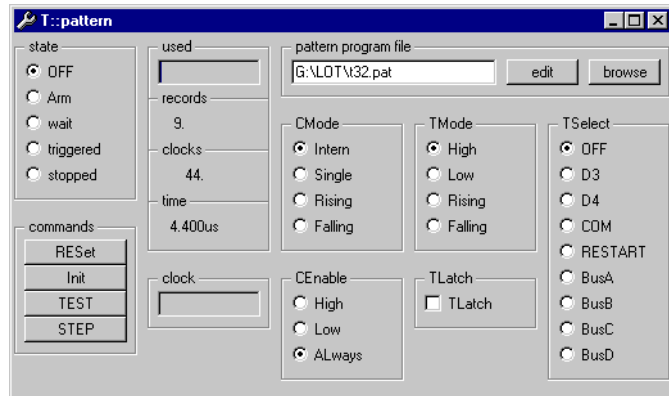
```

- Two retriggerable 48 bit Counters in trigger system
  - Time window definition
- Triggering through bus trigger lines
- Programmable trigger delay 0 to 100% of records
- Triggering of other system units
- Trigger output for oscilloscope etc.

#### Input variables

- Trigger events A,B,C
- Bus trigger lines 0 to 3 (as inputs)
- Event counter actions/operations
- Acquisition ON/OFF
- Trigger
- Bus trigger lines 0...3
- Counter enable
- Counter restart
- Sequential triggering through 8 levels

## Option Pattern Generator



The pattern generator can supply the 16 channels on the connector C and D. A output probe has to be used.

### Channels

- 16 output lines on channel C and D
- 100ns cycle time

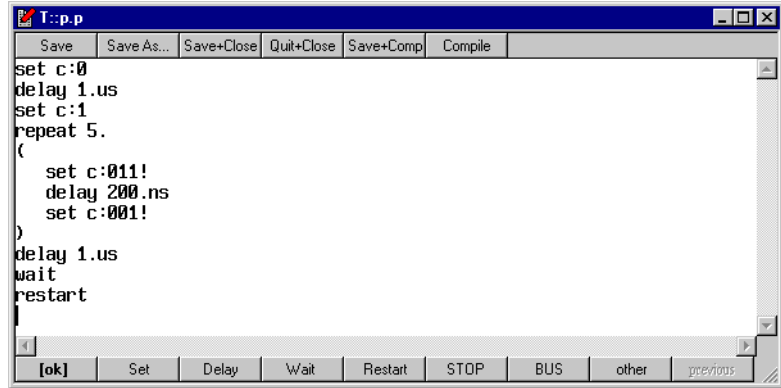
### Trigger

- Trigger latch mode
  - Stores trigger event
- Trigger Input
  - BUS A ...D
  - External D.3
  - External D.4
  - Serial line tester
  - Trigger mode
  - High
  - Low
  - Rising
  - Falling
- Retrigger function
  - Wait for trigger
- Restart trigger output to BUS
  - BUS A ... D

### Clock

- Clock enable input
- External/internal clock
  - 10 MHz internal
  - 0 ...10 MHz external
  - Rising/falling edge
  - Single step
- Clock qualifier
  - High
  - Low
  - Don't care'

## Programming



```

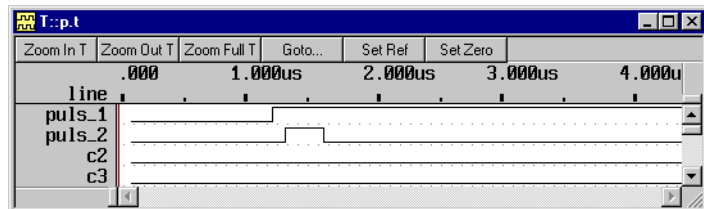
set c:0
delay 1.us
set c:1
repeat 5.
(
  set c:011!
  delay 200.ns
  set c:001!
)
delay 1.us
wait
restart

```

The programming of the pattern generator is done by a text window. Macros can be used for repeating the same sequence several times.

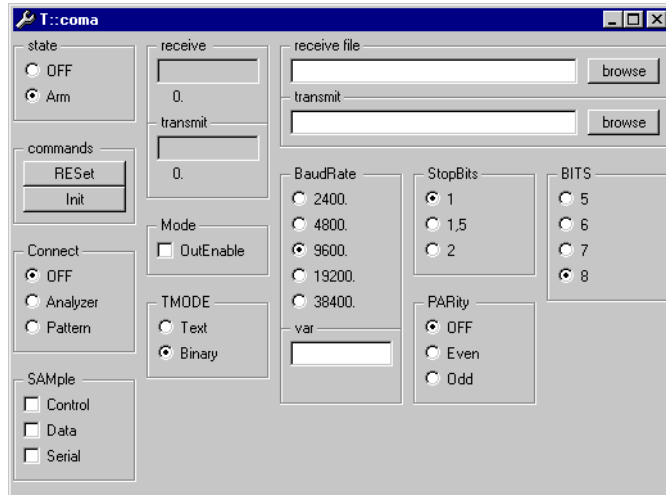
- Pattern Definition
  - Stand-by
  - Set
  - Repeat
  - ()
  - Delay
  - Wait
  - Restart
  - Stop

## Pattern Display



The defined pattern sequence can be displayed as a data listing or a timing diagram.

## Option Serial Line Tester

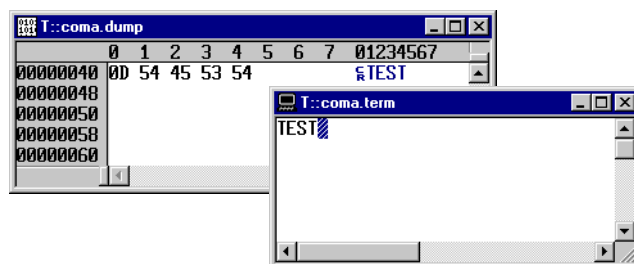


The serial line tester supports 2 channels for asynchronous transfer. Every channel can work together with the timing analyzer, the pattern generator or the file system.

### 2 Channels

- Baudrate
  - 50-76800
- Transfer Mode
  - Even/odd
  - 5...8 bit
  - 1...2 stop bit

### Operation Modes

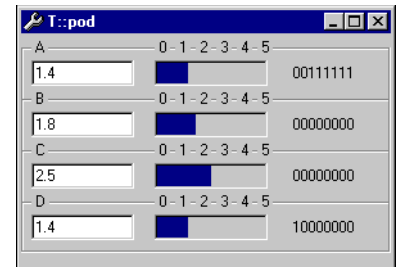


- Terminal operation
- DUMP operation
- Connection to Timing Analyzer
- Connection to Pattern Generator
- File transfer



## Probes

- CREF8
- CIN8
- COUT8
- Clip Set



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## Order Information

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### Module Description

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### Detailed Order Information

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The information presented is intended to give overview information only. Changes and technical enhancements or modifications can be made without notice.