

PowerProbe - Logic and Protocol Analyzer

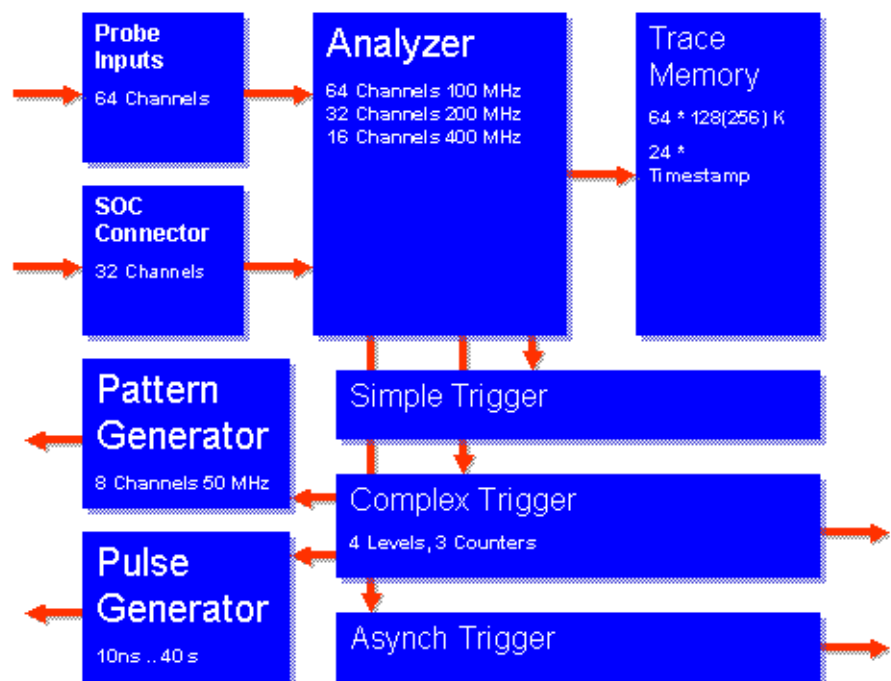
- Timing Analyzer up to 400 MHz
- State Analyzer up to 100 MHz
- 64 Input Channels
- Transient Recording
- Time Correlation with RISC Trace
- Clock Qualifier for State Clock
- Mixed State and Timing Mode
- 4 State Clock Inputs
- Optional FPGA Onchip Trace
- Optional Pattern Generator
- Protocol Support for CAN, USB, etc.

The Timing/State Analyzer Module is special designed for microprocessor applications. It can work separately or in conjunction with all ICD modules. The high-speed transient recording allows very long record time when tracing peripheral lines in a microcontroller application.

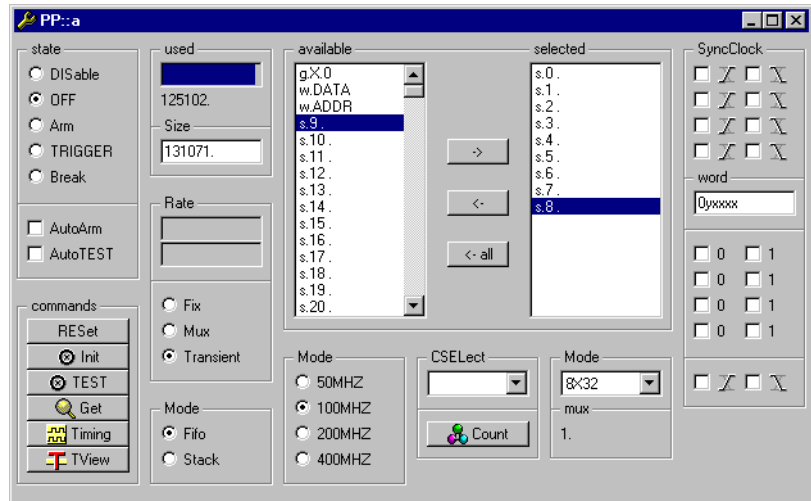
Functional Units

Schematics

PowerProbe



System Features

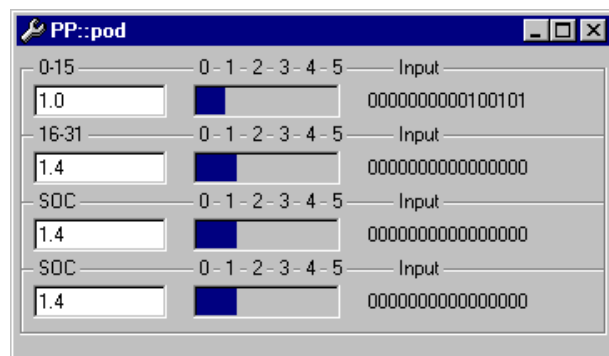


- Timing Analyzer with
 - Trace up to 400 MHz
 - Transient recording
 - Simple trigger function
 - Complex trigger function
- Pattern Generator, which can supply 9 channels with a resolution of 20ns
- SOC Connector
- Pulse Generator
- Universal Counter

Trace

Inputs

- 64 Inputs
- 100 KOhm 7 pF 100 Ohm ser.
- 0..+7.0 V
- 1.0 or 1.4 V threshold level separately definable per group
- 4 groups with 16 lines each
- Probe compensation



Logical names for input Lines

pin	name	pol	configuration
word	w.DATA		s.0 s.1 s.2 s.3 s.4 s.5 s.6 s.
word	w.ADDR		s.8 s.9 s.10 s.11 s.12 s.13 s.
group	g.INT		x.INT0 x.INT1 x.INT2 x.NMI
x.0	x.INT0	-	Transient
x.1	x.INT1	-	Transient
x.2	x.INT2	-	Transient
x.3	x.NMI	-	Transient
x.4	x.4	+	Transient
x.5	x.5	+	Transient
x.6	x.6	+	Transient
x.7	x.7	+	Transient
x.8	x.8	+	Transient
x.9	x.9	+	Transient
x.10	x.10	+	Transient
x.11	x.11	+	Transient
x.12	x.12	+	Transient
x.13	x.13	+	Transient

- Polarity
- Sample Mode
- Groups
- Words

Max. 64 Channels

5 operating modes:

- 64 channels asynchronous 100 MHz
- 32 channels asynchronous 200 MHz
- 16 channels asynchronous 400 MHz
- Up to 32 channels synchronous, 4 clock inputs
- Transient mode

Transient Recording over Required Time

Transient sensitivity can be activated independently for each group. That means, the sampling of the input lines is stored to the trace buffer by the change of the input level only.

The total record time depends on the occurrence of changes on the input signals. The minimum time for high speed signals is 1.2 ms. The max. trace length can be 6.5 h.

Trace Buffer

The depth of the trace buffer is 128K or 256K frames. Each input probe can be used for synchronous or asynchronous events (mixed mode timing/state).

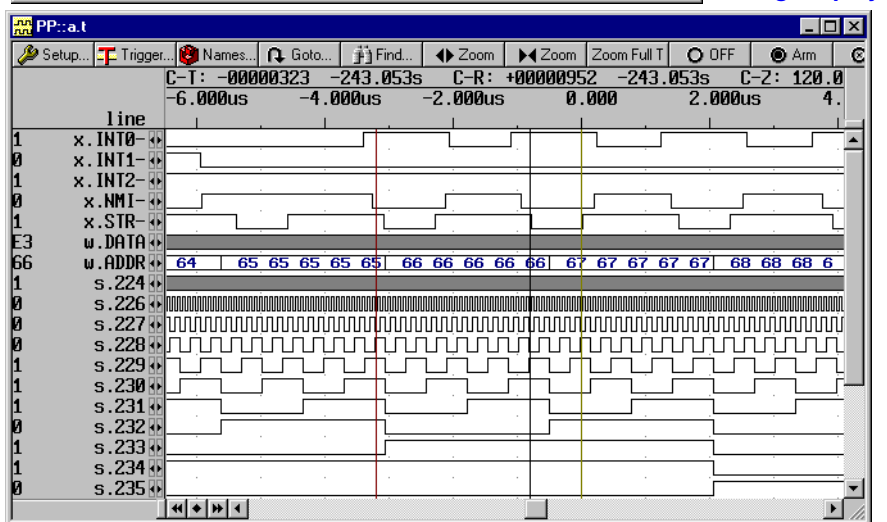
In synchronous mode each recorded frame is marked by a time stamp with a resolution of 10ns.

Display

PP::a.l.g.int.w.data.w.addr.ti.ref

record	int0	int1	int2	.nmi	.str	ta	dr	ti.ref
+00051743						BB	99	-0.013us
+00051744						BB	99	-0.010us
+00051745						BB	99	-0.008us
+00051746						BB	99	-0.005us
+00051747						BB	99	-0.003us
+00051748	-	-	-	-	-	BB	99	0.000
+00051749						BB	99	0.003us
+00051750						BB	99	0.005us
+00051751						BB	99	0.008us
+00051752						BB	99	0.010us
+00051753						BC	99	0.013us
+00051754						BC	99	0.015us
+00051755						BC	99	0.018us
+00051756						BC	99	0.020us
+00051757						BF	99	0.023us
+00051758						BF	99	0.025us
+00051759						BF	99	0.028us
+00051760						BF	99	0.030us
+00051761						BC	99	0.033us
+00051762						BC	99	0.035us

State Display

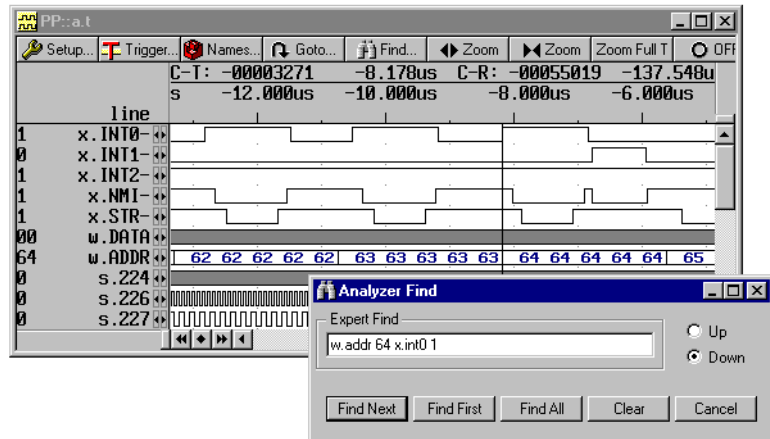


Timing Display

The contents of the trace buffer can be displayed in a tabular form or as a timing

diagram.

Signal Analysis



- LOAD and SAVE
- COMPARE
- FIND
- Tracking

Master-Slave Operation

- The timing analyzer can trigger the other TRACE32 analyzers (high speed state analyzer or port analyzer)
- The timing analyzer can be triggered by the other TRACE32 analyzers.

Output Formats

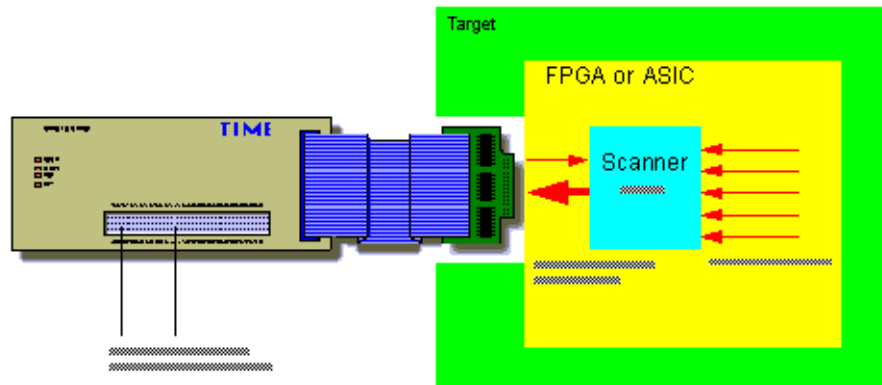
- Binary
- ASCII
- VHDL
- Verilog

Option SOC Adapter

Function

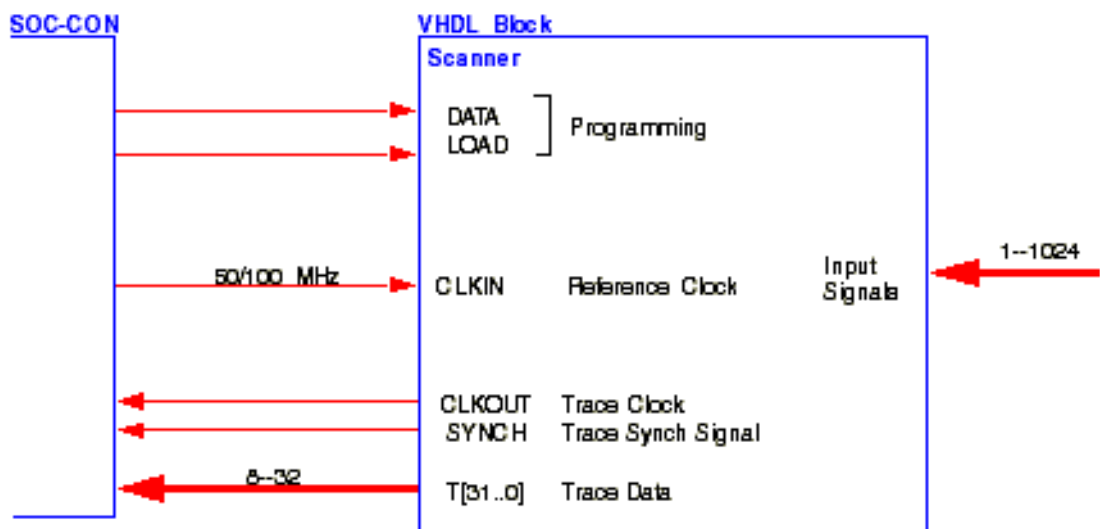
The SOC adaption is a simple way of analyzing internal nodes in FPGAs or ASICS. By integration of a scanner module up to 1024 channels can be

traced inside a silicon system. The SOC adaption is scalable up to 32 multiplexed signals.



Scanner Module

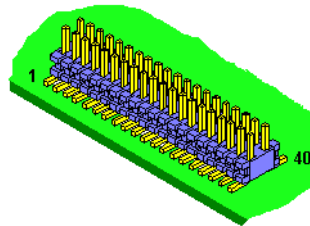
The scanner module is available in VHDL, Verilog or AHDL.



Connector

Connector type is

SAMTEC FTE-120-xxxx



Signals Connector Version A 32 Bit

Signal	Pin	Pin	Signal
GND	1	2	LOAD
DATA	3	4	CLKIN
CLKOUT	5	6	SYNCH
T00	7	8	T01
T02	9	10	T03
T04	11	12	T05
T06	13	14	T07
GND	15	16	VCC
T08	17	18	T09
T10	19	20	T11
T12	21	22	T13
T14	23	24	T15
T16	25	26	T17
T18	27	28	T19
T20	29	30	T21
T22	31	32	T23
T24	33	34	T25
T26	35	36	T27
T28	37	38	T29
T30	39	40	T31

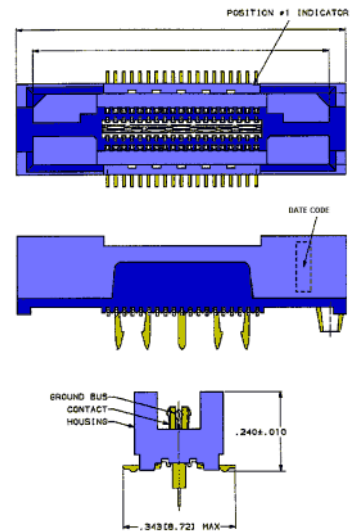
Signals Connector Version A 16 Bit

Signal	Pin	Pin	Signal
GND	1	2	LOAD
DATA	3	4	CLKIN
CLKOUT	5	6	SYNCH
T00	7	8	T01
T02	9	10	T03
T04	11	12	T05
T06	13	14	T07
GND	15	16	VCC
T08	17	18	T09
T10	19	20	T11
T12	21	22	T13
T14	23	24	T15

Signals Connector Version A 8 Bit

Signal	Pin	Pin	Signal
GND	1	2	LOAD
DATA	3	4	CLKIN
CLKOUT	5	6	SYNCH
T00	7	8	T01
T02	9	10	T03
T04	11	12	T05
T06	13	14	T07
GND	15	16	VCC

Connector MICTOR



Signal Connector Version B (MICTOR)

Signal	Pin	Pin	Signal
VCC	1	2	LOAD-
CLKIN	3	4	DATA
CLKOUT	5	6	SYNCH
T15	7	8	T31
T14	9	10	T30
T13	11	12	T29
T12	13	14	T28
T11	15	16	T27
T10	17	18	T26
T09	19	20	T25
T08	21	22	T24
T07	23	24	T23
T06	25	26	T22
T05	27	28	T21
T04	29	30	T20
T03	31	32	T19
T02	33	34	T18
T01	35	36	T17
T00	37	38	T16

Complex Trigger System (optional)

Trigger

- Trigger Conditions
 - HIGH, LOW or DONTCARE for each input
 - Range trigger definitions for each group
- 8 Trigger Events
 - 8 global event, no death time
- Trigger Filter

Freely programmable Trigger Sequencer

```

a.p
Save Save As... Save+Close Quit+Close Save+Comp Compile
DATA chipselect_1 a:011111110! b:34
DATA chipselect_2 datstr b:34
EVENT delay 1000.

COUNT delay if datstr:a:chipselect_1
GOTO trigg if delay

trigg:
BREAK if chipselect_2

GOTO CONTinue Sample. OUT. Count. other previous
  
```

Input variables

- Trigger events from input
- Bus trigger lines A
- Event counter actions/operations
- Acquisition ON/OFF
- Trigger
- Bus trigger lines A
- Counter enable
- Counter restart
- Sequential triggering through 4 levels

- Programmable trigger delay 0 to 100% of records
- Triggering of other system units

Pretrigger Delay

The pretrigger delay prevents from immediate triggering which generates an nearly empty trace storage. The value can be defined between 0 and 100% of the trace storage.

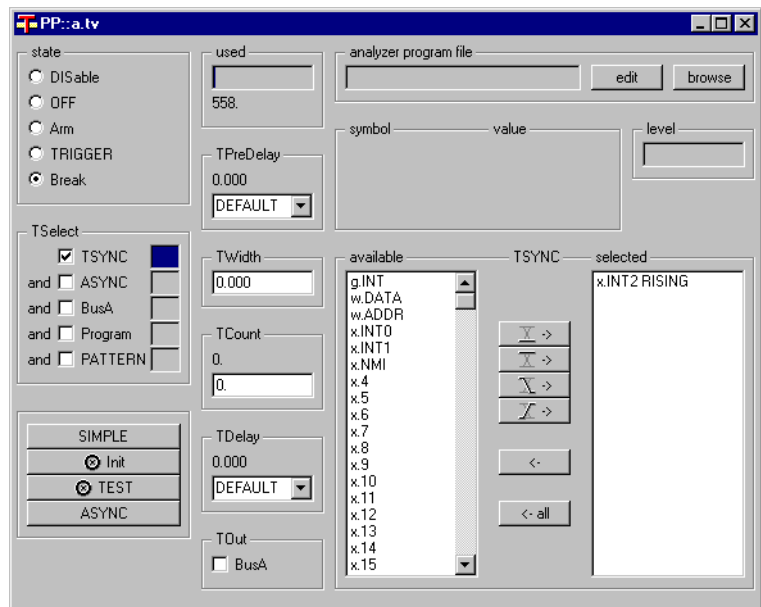
Trigger Delay

The trigger delay can be 0 to 100 s or 0 to 1000% of the trace storage.

- 3 retriggerable 45 bit Counters in trigger system
 - Time window definition
- Triggering through bus trigger lines

Simple Trigger

Function



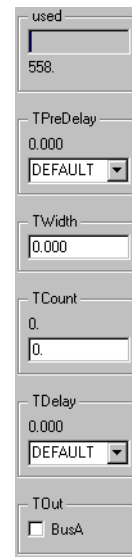
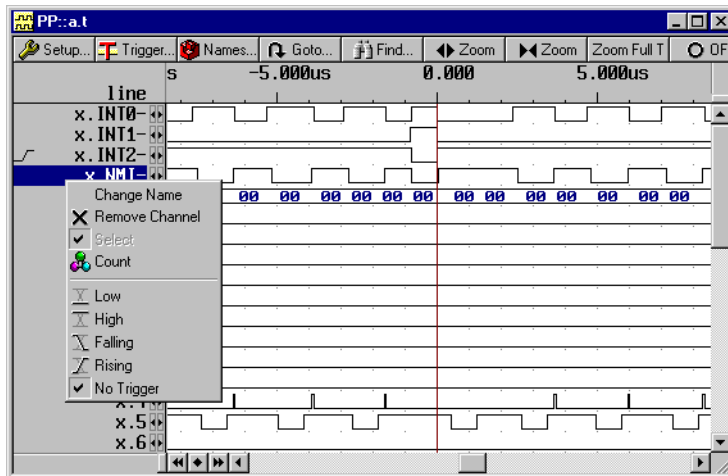
The simple trigger systems brings the easy trigger function of a scope to the logic analyzer. Trigger conditions can be set by mouse without any keyboard interaction.

Trigger Comparator

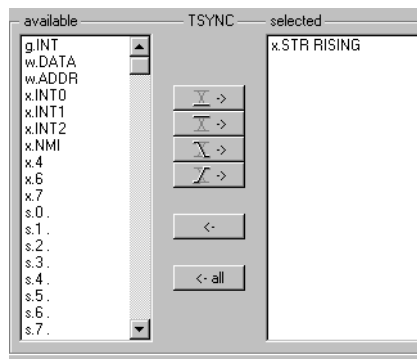
Every input can be used as high, low, rising or falling edge. More than one edge can be combined to generate a valid trigger event.

- Trigger Events
 - Don't care
 - Low
 - High
 - Rising
 - Falling

Direct setting with mouse



Selection Menu



Other Trigger Inputs

- Intertrigger Bus
 - BUS A
- Asynchronous Trigger
- Pattern Generator

Trigger Filters

Trigger Filter

The trigger filter can filter out glitches or runts on the lines. The trigger filter can be set from 0 to 2.5 us.

Trigger Counter

The trigger count can be defined from 0 to 16 Mio. trigger events

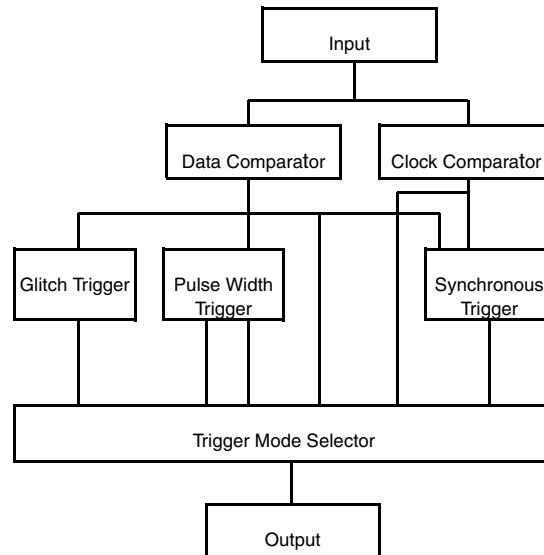
Pretrigger Delay

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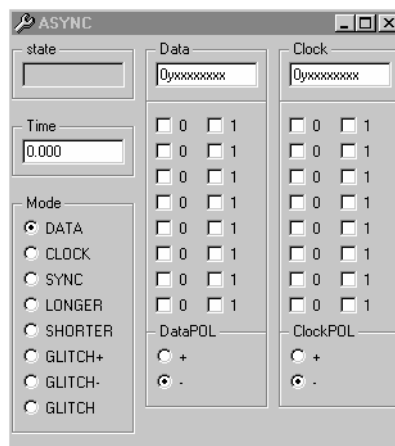
Trigger Delay

The trigger delay can be 0 to 100 s or 0 to 1000% of the trace storage.

Asynchronous Trigger System



The asynchronous trigger system can be used to trigger on high-speed events, which are not synchronous to the CPU clock or bus cycle. The trigger reacts on events shorter than 3 ns.



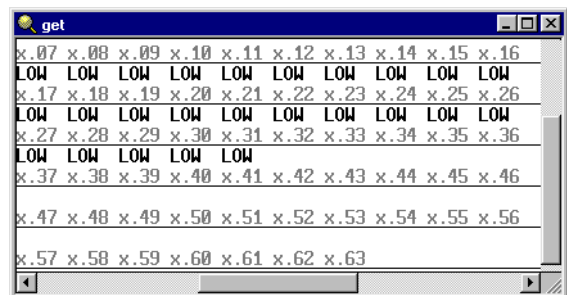
The trigger output can be used to trigger the port analyzer, the emulator or switched to the frequency counter. Events up to 100 MHz can be measured.

- Data
 - Combines 8 Inputs to one trigger signal
 - High, Low, Don't Care for every bit
 - Positive and negative polarity for trigger output
- Clock
 - Same as Data, but 2nd comparator
- SYNC
 - Combination of Data and Trigger event
 - Positive and negative Clock edge
 - True and false data event
- LONGER
 - Pulse width trigger
 - 10ns .. 3 ms
 - Positive and negative pulse
- SHORTER
 - Pulse width trigger
 - 10ns .. 3 ms
 - Positive and negative pulse
- GLITCH+
 - Glitch trigger on positive pulse
 - 2..10ns detection
- GLITCH-
 - Glitch trigger on negative pulse
 - 2..10ns detection

- GLITCH
 - Glitch trigger on positive or negative pulse
 - 2..10ns detection

Activity Display

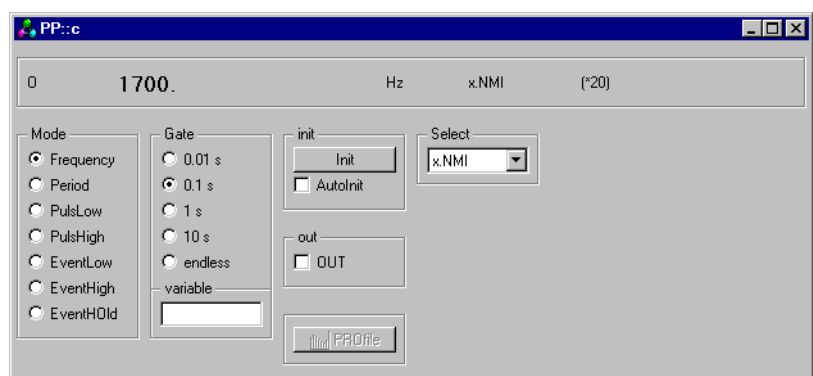
Every port or external line level or pulse activity can be displayed.



Counter System

Every signal can be selected for the universal counter system on the Trace32 FIRE. Event count and pulse width measurement is possible as well

a frequency test on CPU signals. On external inputs up to 100 MHz for input clocks is possible (Frequency only).



Pulse Generator

Rate Generator

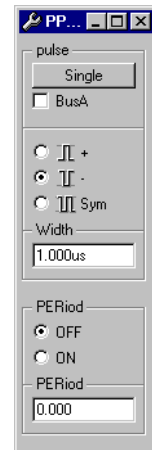
10 ns .. 40s

Pulse Width

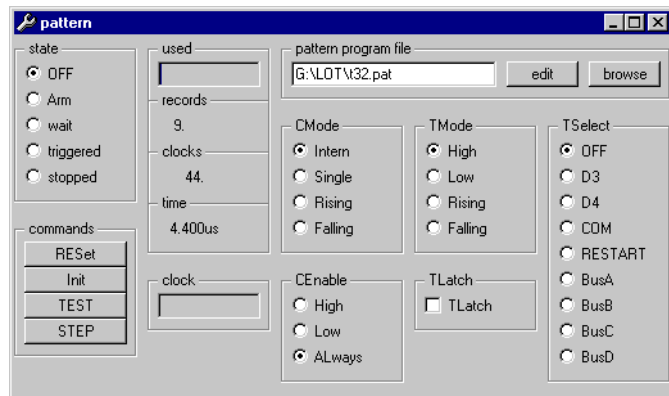
10ns .. 40s

Trigger

- Extern
- Analyzer Trigger
- BUS A
- Pattern Generator



Option Pattern Generator



The pattern generator can supply the 16 channels on the connector C and D. A output probe has to be used.

Channels

- 9 output lines on AUX0 .. AUX8
- 20 ns cycle time

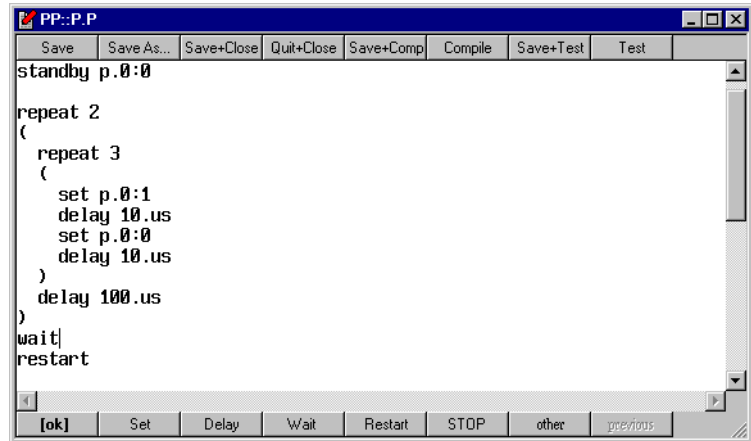
Trigger

- Trigger latch mode
 - Stores trigger event
- Trigger Input
 - BUS A
 - External 4 Lines
- Trigger mode
 - High
 - Low
 - Rising
 - Falling
- Retrigger function
 - Wait for trigger
- Restart trigger output to BUS
 - BUS A

Clock

- Clock enable input
- External/internal clock
 - 50 MHz internal
 - 0 ...50 MHz external
 - Rising/falling edge
 - Single step
- Clock qualifier
 - High
 - Low
 - Don't care'

Programming



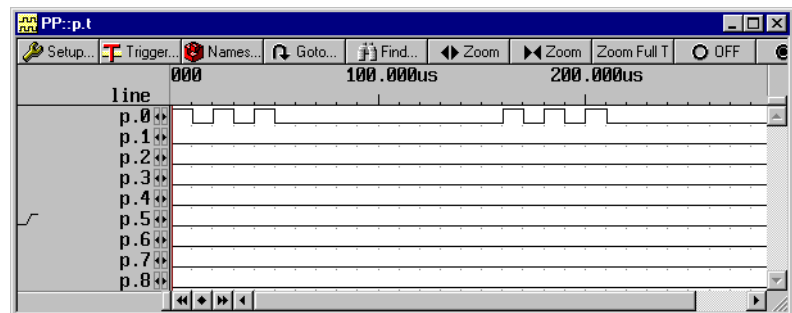
```

PP::P.P
Save Save As... Save+Close Quit+Close Save+Comp Compile Save+Test Test
standby p.0:0
repeat 2
(
repeat 3
(
set p.0:1
delay 10.us
set p.0:0
delay 10.us
)
)
delay 100.us
)
wait
restart
[ok] Set Delay Wait Restart STOP other previous
  
```

The programming of the pattern generator is done by a text window. Macros can be used for repeating the same sequence several times.

- Pattern Definition
 - Stand-by
 - Set
 - Repeat
 - ()
 - Delay
 - Wait
 - Restart
 - Stop

Pattern Display



The defined pattern sequence can be displayed as a data listing or a timing diagram.

Order Information

Module Description

OrderNo Code	Text
LA-7930 ICD-PP	ICD PowerProbe State-Timing Analyzer 128K ICD State-Timing Analyzer, 64 Channels 100 MHz, 32 Channels 200 MHz, 16 Channel 400 MHz, Transient Recording, 128 KFrames, 48 Bit Time-Stamp, Trigger Filter, Trigger Delay, etc. Requires PODBUS-Interface, No SOC-CON Support
LA-7931 ICD-PP-256K	ICD PowerProbe State-Timing Analyzer 256K ICD State-Timing Analyzer, 64 Channels 100 MHz, 32 Channels 200 MHz, 16 Channels 400 MHz, Transient Recording, 256 KFrames, 48 Bit Time-Stamp, Complex Trigger, 8 Trigger Events, 4 Trigger Levels, 3 Counters (45 bit), Trigger Filter, Trigger Delay, etc., 50 MHz Pattern Generator (9 bit), Requires PODBUS-Interface, Option for SOC Trace
LA-7933 ICD-PP- EXCALIBUR	Adapter EXCALIBUR / SOC-CON Converter EXCALIBUR (200 pin) to SOCCON (MICTOR)
LA-7649 CONV-MIC38- 2.54MM	Converter Mictor38 to 2.54 mm Connector Converter from Mictor 38 to 2.54 mm Connector

Detailed Order Information

Order No.	Code	Text
LA-7930	ICD-PP	ICD PowerProbe State-Timing Analyzer 128K
LA-7931	ICD-PP-256K	ICD PowerProbe State-Timing Analyzer 256K
LA-7933	ICD-PP- EXCALIBUR	Adapter EXCALIBUR / SOC-CON
LA-7649	CONV-MIC38- 2.54MM	Converter Mictor38 to 2.54 mm Connector
Additional Options		
LA-6470	CLIPSET	Clip Set (Cable and Clips)

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