



In-Circuit Emulator for 80196

- Bondout support
- Works with Intel, Tasking and IAR Compilers
- C++ support
- Dual ported memory
- Banking support for 256 banks
- Supports memory split for program and data
- CASE tools interface
- RTOS support
- Software compatible ROM Monitor
- Windows95, NT and X windows interface

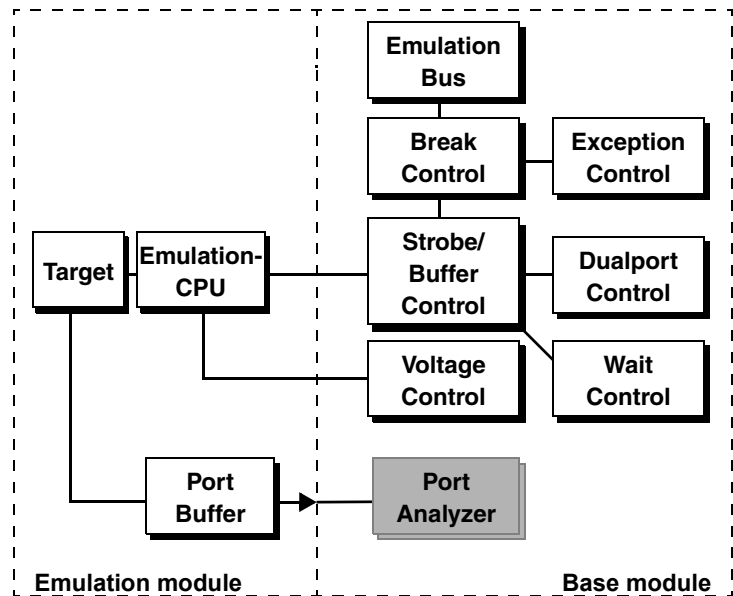
8XC196EN

The TRACE32-ICE196 supports bondout microcontroller from Intel. Its modular and open technology allows the fast integration of new chip designs.

A software compatible SDU Debugger is available for the 196EA. All other derivatives are supported by a ROM Monitor.

TRACE32 works with the highest variety of host interfaces. The communication link to the host is done by the printer port, a fibre optic interface or ethernet allowing a high-speed transfer.

Basics of Operation



The ICE-196 is a high-performance emulation system for most of the members of the 196 family from Intel.

On the emulation base there is an extra slot for the TRACE32 Port Analyzer. Depending on CPU type various signals can be traced. Some probes have connectors to trace external target lines.

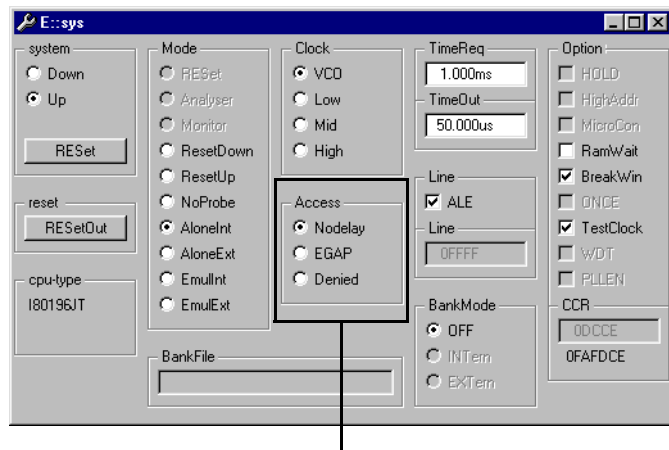
Operating Modes

The Emulator can work in stand-alone mode with internal clock or in active mode with internal or the target clock. On power-down of the target system the emulator tristates its output buffers and isolates its internal emulation circuits.

The operation modes are as follows:

- Reset Down
- Reset Up
- No Probe
- Alone Internal
- Alone External
- Emulation Internal
- Emulation External

Dual-Port Access



Dual port access modes

All TRACE32 memories are dual-ported. The dual-port access makes it possible to display and modify the contents of the overlay memory, to set or delete breakpoints or use the flag memory while the application is running in real-time.

The following dual-port access modes are implemented:

- Nodelay
- EGAP

In the **Nodelay mode** the dual-port cycle is inserted between the bus cycles generated by the CPU. This

means that the max. speed of operation is not possible in this mode, or extra wait states are needed for correct operation.

In the **EGAP mode** the dual-port cycle is inserted between the bus cycles generated by the CPU. This means that the max. speed of operation is not possible in this mode, or extra wait states are needed for correct operation. EGAP mode is working with higher frequencies, but flag system is disabled in this mode.

In the **Denied mode** the dual port access is switched off.

Max. Operation Frequency

- 20
- 16/32 MHz for the 196EA

Clock

- Operation with external or internal clock
- 1..40 MHz internal clock

HLL Debugging

Step	Step Over	Go Next	Go Return	Go Up	Go	Break	Mode
addr/line	code	label	mnemonic	comment			
		int anzahl;					
665		anzahl = 0;					
P:002CE5	C31A0200		st	0,2[1A]	; R0,anzahl		
667		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;					
P:002CE9	0124		clr	24			
P:002CEB	200D		sjmp	2CFA			
P:002CED	A0241C		ld	1C,24	; FP0_FRAC,		
P:002CF0	0724		inc	24			
P:002CF2	B1011E		ldb	1E,#1			
P:002CF5	C71D3382		stb	1E,8233[1C]	; 1E,FLAGSI		
P:002CFA	89120024		cmp	24,#12	; 24,#IPEND		
P:002CFE	DAED		jle	2CED			
669		= SIZE ; i++)					
P:002D00	0124		clr	24			
P:002D02	2030		sjmp	2D34			

The TRACE32 Debugger support all standard compiler for C and PLM from Intel. For more information on the supported compilers refer to the section "Debug Interfaces".

Full support in real-time for:

- Break-before-line operation
- HLL single step in real-time
- Trigger and trace on local variables

Background Task

The background task allows:

- To process interrupts

- To maintain the refresh of a target DRAM while the emulation is stopped.

Wait System

- Additional wait cycles (1-15) may be specified
- Up to 250 wait cycles (4K blocks globally and bitwise)

Banking Support

External bank switching schemes can be supported by the memory mapper. Therefore a separate input probe is needed for the emulator.

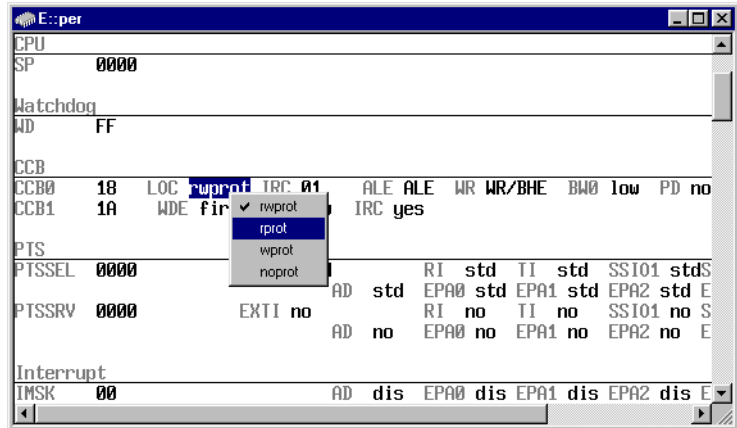
Page EPROMs are also supported by memory mapper.

Selective Mapping of Memory Classes

The address mapper can segment the memory into program and data area. By using this segmentation e.g. it is

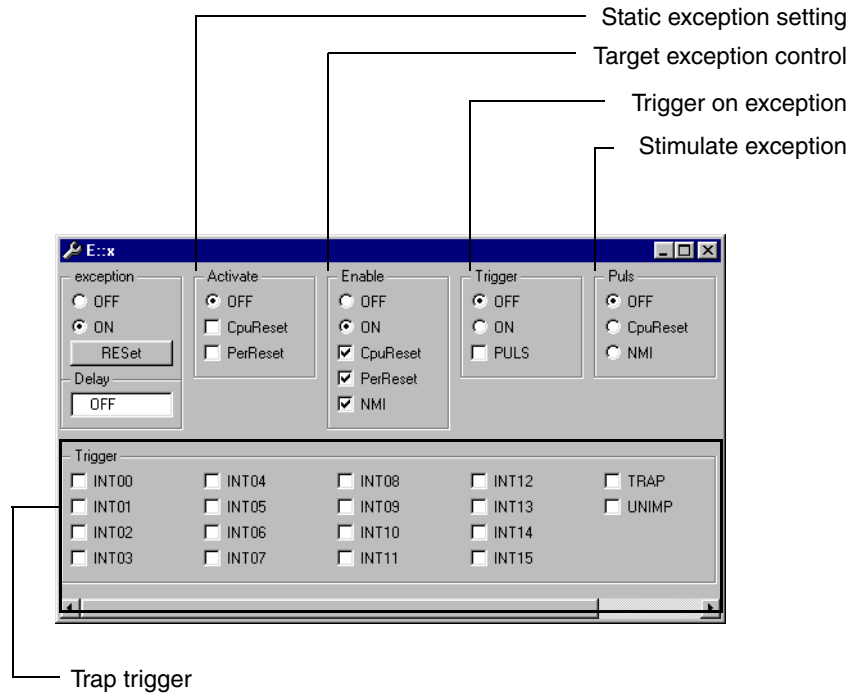
possible to map the program area to the emulation memory while the RAM area remains mapped to the target.

CPU Peripherals



- Display of onchip peripherals
- User definable display of the onchip peripherals
- Definition is done interactive supported by softkeys
- Pull down menus for settings
- Additional description for each field
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-

Exception Control



The TRACE32 exception controller allows to permanently activate an exception, to enable or disable specific

exceptions, to trigger on specific exceptions or to stimulate an exception.

Clock Fail Detection

On-Circuit Emulation

- Supports ONCE mode for Clip-Over adaptation.

Modules Overview

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Debug Interfaces

TRACE32-PowerView supports most compilers, realtime operation systems and debuggers.

New integrations are mostly done on customers request. If your compiler or RTOS is not supported now, please ask us !

Compiler Support 196

CPU	Language	Compier	Compan y	Option
80196	C	ICC196	IAR Systems AB	UBROF
80196	C	IC96	Intel Corporation	OMF-96
80196	C	C196	TASKING	OMF-96
80196	PLM	PL/M96	Intel Corporation	OMF-96

RTOS Support

Debugger Support

CPU	Debugger	Company
	WINDOWS CE PLATF. BUILDER	-
	CODE::BLOC KS	-
	C++TEST	-
	ADENEO	-
	X-TOOLS / X32	blue river software GmbH
	CODEWRIGH T	Borland Software Corporation
	CODE CONFIDENC E TOOLS	Code Confidence Ltd
	CODE CONFIDENC E TOOLS	Code Confidence Ltd
	EASYCODE	EASYCODE GmbH
	ECLIPSE	Eclipse Foundation, Inc
	CHRONVIEW	Inchron GmbH
	LDRA TOOL SUITE	LDRA Technology, Inc.
	UML DEBUGGER	LieberLieber Software GmbH
	SIMULINK	The MathWorks Inc.
	ATTOL TOOLS	MicroMax Inc.
	VISUAL BASIC INTERFACE	Microsoft Corporation
	LABVIEW	NATIONAL INSTRUMENT S Corporation
	RAPITIME	Rapita Systems Ltd.
	RHAPSODY IN MICROC	IBM Corp.

CPU	Debugger	Company
	RHAPSODY IN C++	IBM Corp.
	DA-C	RistanCASE
	TRACEANALY ZER	Symtavigation GmbH
	TA INSPECTOR	Timing Architects GmbH
	UNDODB	Undo Software
	VECTORCAS T UNIT TESTING	Vector Software
	VECTORCAS T CODE COVERAGE	Vector Software

Operation Voltage and Frequency

The maximum operation frequency of TRACE32-ICE depends on:

- The max. frequency of the CPU
- The access time of the overlay memory (15ns or 35ns)
- The mapper mode (**S**low or **F**ast)
- The number of waitstates (W0 = 0 waitstates
W1 = 1 waitstate)
- The dual-port access mode

Denied Access

Nodelay Access

Operating Voltage

This list contains information on probes available for other voltage ranges.

Probes not noted here supply an operation voltage range from 4.5V to 5.5V. tbd

Dimensions

Module Dimensions

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Connectors

On each emulation module there are half-size connectors to:

- ❑ Connect the emulation module directly to the target by providing the corresponding connectors also on the target hardware

- ❑ Connect a standard adapter from Emulation Technology, YAMAICHI, AMP, TOKYO ELETECH etc.

The following table lists the physical dimensions of these connectors.

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Adapter

The adapters connect in different ways

- With Clip-Over Adapters the CPU can stay on the target board.
- With Solder-ON adapters the CPU must be removed

- YAMAICHI and AMP adapters fit to the CPU socket

The following table lists the physical dimensions of these adapters.

Not necessary.

Available Tool Chain

TRACE32 provides a complete set of development tools for this family. This includes:

- The In-Circuit Emulator TRACE32-ICE
- The high speed RISC Emulator TRACE32-FIRE
- The BDM/JTAG/ONCE etc. based In-Circuit Debugger TRACE32-ICD
- The ROM Monitor based In-Circuit Debugger TRACE32-ICD
- The ICD Trace, a trace extension to the BDM/JTAG debuggers or ROM monitors
- Evaluation boards, which can be used until the target hardware is available.
- The Instruction Set Simulator (SIM), a software tool for code test without any hardware

The following list give an overview which development tools are available for the specific derivatives of this family.

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Module Description

Detailed Order Information

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