

In-Circuit Emulator for 68HC11

MC68HC11A
 MC68HC11C
 MC68HC11D
 MC68HC11E
 MC68HC11F
 MC68HC11G
 MC68HC11K
 MC68HC11KA
 MC68HC11KW
 MC68HC11N
 MC68HC11P
 MC68HC11PH
 MC68HC711D
 MC68HC711E
 MC68HC711K
 MC68HC711KA
 MC68HC711P
 MC68HC811E

- Modular design for up to 6 MHz
- Support for 5V and 3.3V
- Banking and MMU support
- Support for single chip and expanded mode
- On chip EEPROM access
- Support for test modes
- Trace and trigger on internal accesses
- Bootloader support
- Support for all compilers
- Available as cost effective TRACE32-COMPACT
- Windows9x, NT and X windows interface

The ICE-11 probe is a high-performance emulation system for many derivatives of the 68HC11 family including the CPUs with MMU. The change between different CPU types is done by changing the adapter board.

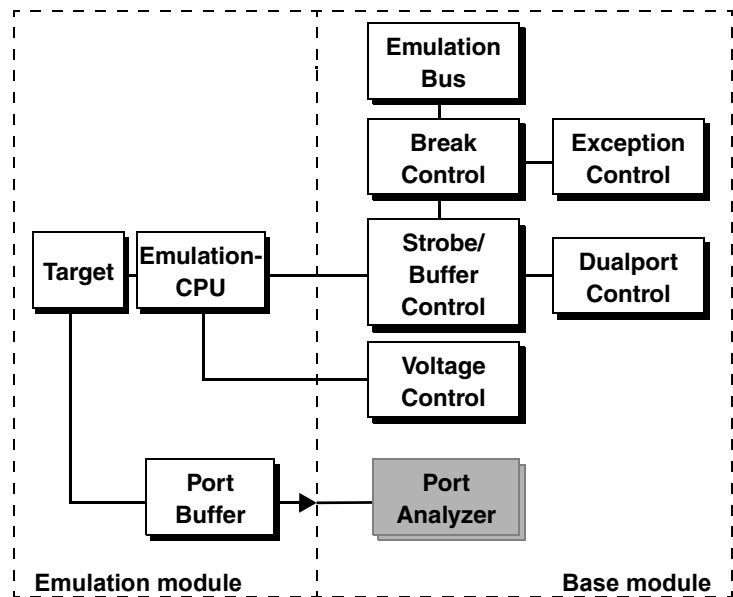
The probe supports high-speed emulation. The CPU can be emulated in single chip or expanded mode. The test mode is available for both modes. The emulator can support up to 256 banks. Internal access to RAM or peripherals can be traced and triggered.

As internal address bus is 20 bit the K4 version may be supported with or without MMU.

TRACE32 for the 68HC11 family is available as an 8-bit compact solutions and as 32-bit emulation system.

Features

Basics of Operation



The ICE 11 probe is a high-performance emulation system for many derivatives of the 68HC11 family. The change between different CPU types is done by changing the adapter board. The probe supports high-speed emulation and external

bank systems. It runs together with the 8 bit controller ECC8 or the 32 bit controller ECU32. As internal address bus is 20 bit the K4 version may be supported with or without MMU.

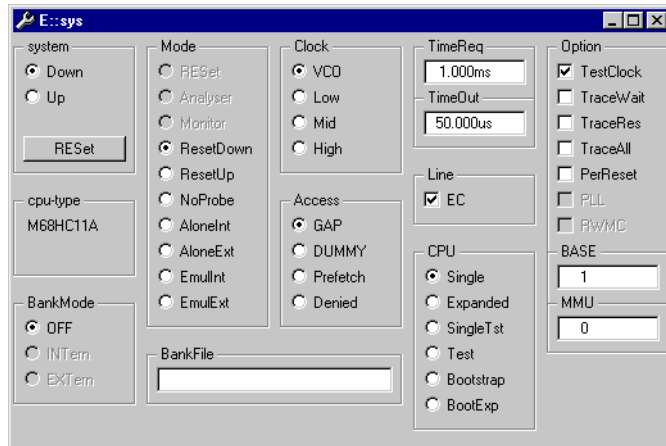
Operating Modes

- | | |
|---|---|
| <input type="checkbox"/> Reset Down | <input type="checkbox"/> Alone External |
| <input type="checkbox"/> Reset Up | <input type="checkbox"/> Emulation Internal |
| <input type="checkbox"/> No Probe | <input type="checkbox"/> Emulation External |
| <input type="checkbox"/> Alone Internal | |

Max. Operation Frequency

- 6 MHz (24 MHz clock)

Emulation Modes



- Single-Chip
- Expanded
- Test
- Single Test
- Bootstrap

Internal Clock 0.75 to 25 MHz

Multitask Debugging

- 1 foreground task
- 1 background task

Trace Control

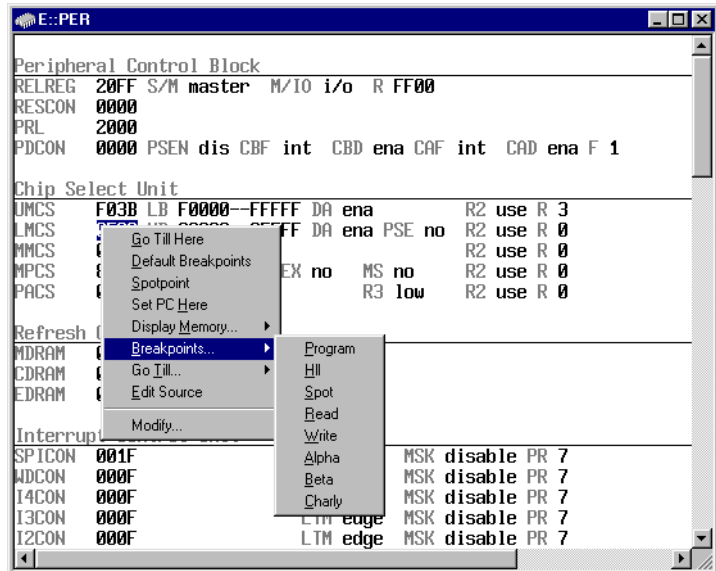
- TraceReset
- TraceWait
- TraceAll

By default no prefetch or idle cycles are traced

Voltage and Clock Monitors for the Target System

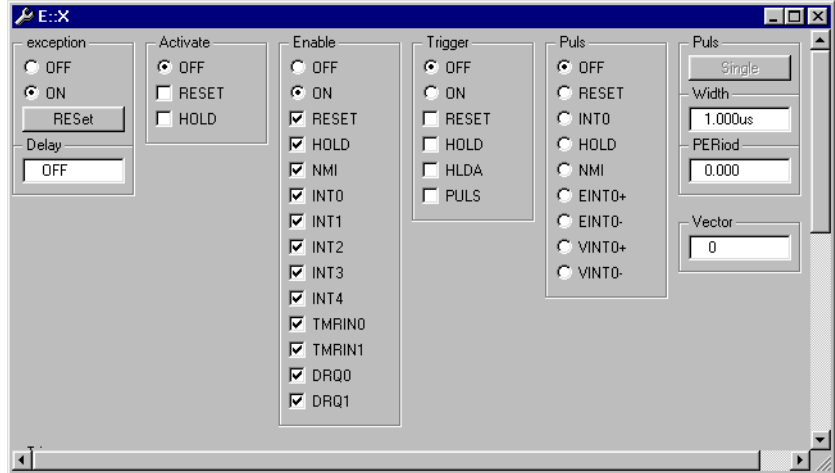
- Clock monitor may be swichted off

Peripheral Window



- Display of onchip peripherals
- User definable display of the onchip peripherals
- Definition is done interactive supported by softkeys
- Pull down menus for settings
- Additional description for each field
-

Exception Control



Exception system is used to control and simulate all special CPU lines like RESET or interrupt inputs. This is especially useful during the development phase, allowing to disable CPU input lines, or to simulate certain events.

- Static Exception Setting
 - Reset
- Target Exception Control
 - Reset
 - IRQ
 - XIRQ

- Exception Trigger
 - Reset
 - IRQ
 - XIRQ
 - Simulation
- Exception Simulation
 - Reset
 - IRQ
 - XIRQ

Memory Banking

TRACE32 supports up to 256 64K banks. The following bank modes are supported:

- Off

- Probe (external)
- EPROM (internal)
- MMU support for K4 version

EEPROM Support

- EEPROM may be loaded or erased directly (monitor based EEPROM write function)

Real-Time Cycle Sequencing

TRACE32-ICE11 uses a special code sequencer to classify CPU bus cycles on realtime emulation. This feature

allows perfect trigger and trace functions as prefetch cycles or idle cycles are not traced.

record	run	address	cycle	.b
000023	f	D:006849	pfetch	37
000022	f	D:002415	dummy	02
000021	f	D:002416	rd-stk	69
000020	f	D:002417	rd-stk	A2
000019	f	P:0069A2	opfetch	38
000018	f	D:0069A3	pfetch	F7
000017	f	D:002417	dummy	A2
000016	f	D:002418	rd-stk	00
000015	f	D:002419	rd-stk	03
000014	f	P:0069A3	opfetch	F7
000013	f	P:0069A4	sfetch	20
000012	f	P:0069A5	sfetch	2A
000011	f	D:00202A	wr-mem	05
000010	f	P:0069A6	opfetch	01
500				
501			while (TRUE)	
000009	f	D:0069A7	pfetch	8D
000008	f	P:0069A7	opfetch	8D
000007	f	P:0069A8	sfetch	02
502			{	

Without Sequencer

- Functional stamps on all cycles
- No trace of prefetch or idle cycles
- Internal/external stamp
- Stack/data stamp
- Normal/exception cycle stamp

record	run	address	cycle	.b
000023	f	D:006849	pfetch	37
000022	f	D:002415	dummy	02
000021	f	D:002416	rd-stk	69
000020	f	D:002417	rd-stk	A2
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With Sequencer

- Wait cycle stamp
- No trigger on prefetch cycles
- No flag setting on prefetch cycles
- Protection data/programm

Power Consumption

- 6 W

Modules Overview

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Debug Interfaces

TRACE32-PowerView supports most compilers, realtime operation systems and debuggers.

New integrations are mostly done on customers request. If your compiler or RTOS is not supported now, please ask us !

Compiler Support

CPU	Language	Compier	Compan y	Option
68HC11	ASM	A6801	IAR Systems AB	UBROF
68HC11	C	CX68HC11	Cosmic Software	COSMIC
68HC11	C	GCC11	GNU Compiler Collectio n	DBX
68HC11	C	ICC6811	IAR Systems AB	UBROF
68HC11	C	C11	Introl Corporati on	ICOFF
68HC11	C	HICROSS-C	NXP Semicon ductors	HICROSS
68HC11	C	CC11	NXP Semicon ductors	COFF

RTOS Support

Company	Product	Comment
Enea OSE Systems	OSE Basic	(OS11)
-	OSEK	via ORTI
Elektrobit Automotive GmbH	ProOSEK	via ORTI

Debugger Support

CPU	Debugger	Company
	WINDOWS CE PLATF. BUILDER	-
	CODE::BLOC KS	-
	C++TEST	-
	ADENEO	-
	X-TOOLS / X32	blue river software GmbH
	CODEWRIGH T	Borland Software Corporation
	CODE CONFIDENC E TOOLS	Code Confidence Ltd
	CODE CONFIDENC E TOOLS	Code Confidence Ltd
	EASYCODE	EASYCODE GmbH
	ECLIPSE	Eclipse Foundation, Inc
	CHRONVIEW	Inchron GmbH
	LDRA TOOL SUITE	LDRA Technology, Inc.
	UML DEBUGGER	LieberLieber Software GmbH
	SIMULINK	The MathWorks Inc.
	ATTOL TOOLS	MicroMax Inc.
	VISUAL BASIC INTERFACE	Microsoft Corporation
	LABVIEW	NATIONAL INSTRUMENT S Corporation
	RAPITIME	Rapita Systems Ltd.
	RHAPSODY IN MICROC	IBM Corp.

CPU	Debugger	Company
	RHAPSODY IN C++	IBM Corp.
	DA-C	RistanCASE
	TRACEANALY ZER	Symtavigation GmbH
	TA INSPECTOR	Timing Architects GmbH
	UNDODB	Undo Software
	VECTORCAS T UNIT TESTING	Vector Software
	VECTORCAS T CODE COVERAGE	Vector Software

Operation Voltage and Frequency

The maximum operation frequency of TRACE32-ICE depends on:

- The max. frequency of the CPU
- The access time of the overlay memory (15ns or 35ns)
- The mapper mode (**S**low or **F**ast)
- The number of waitstates (W0 = 0 waitstates
W1 = 1 waitstate)
- The dual-port access mode

Denied/Dummy/Prefetch Access

Operation Voltage

This list contains information on probes available for other voltage ranges. Probes not noted here supply an operation voltage range from 4.5V to 5.5V.

Other probes for 3.3V can be delivered on request.
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Dimensions

Module Dimensions

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Connectors

On each emulation module there are half-size connectors to:

- ❑ Connect the emulation module directly to the target by providing the corresponding connectors also on the target hardware

- ❑ Connect a standard adapter from Emulation Technology, YAMAICHI, AMP, TOKYO ELETECH etc.

The following table lists the physical dimensions of these connectors.

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Adapter

The adapters connect in different ways

- With Clip-Over Adapters the CPU can stay on the target board.
- With Solder-ON adapters the CPU must be removed

- YAMAICHI and AMP adapters fit to the CPU socket

The following table lists the physical dimensions of these adapters.

Not necessary.

Available Tool Chain

TRACE32 provides a complete set of development tools for this family. This includes:

- The In-Circuit Emulator TRACE32-ICE
- The high speed RISC Emulator TRACE32-FIRE
- The BDM/JTAG/ONCE etc. based In-Circuit Debugger TRACE32-ICD
- The ROM Monitor based In-Circuit Debugger TRACE32-ICD
- The ICD Trace, a trace extension to the BDM/JTAG debuggers or ROM monitors
- Evaluation boards, which can be used until the target hardware is available.
- The Instruction Set Simulator (SIM), a software tool for code test without any hardware

The following list give an overview which development tools are available for the specific derivatives of this family.

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Module Description

Detailed Order Information

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Disclaimer

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