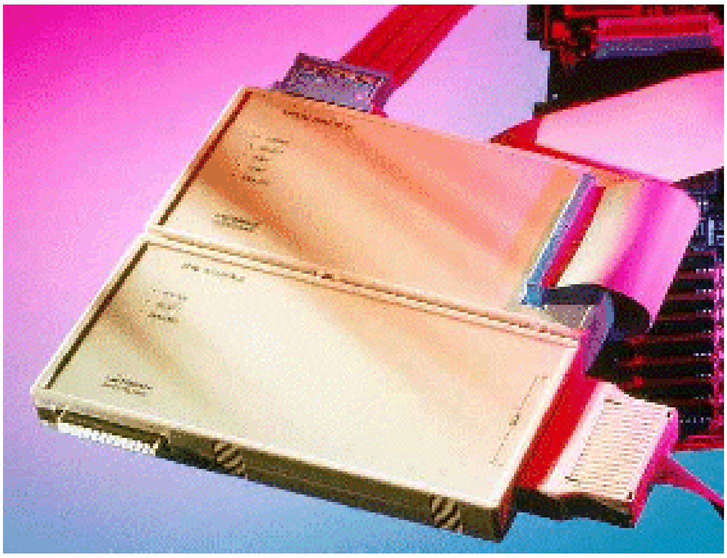
TRACE32®
Technical Information



ICD In-Circuit Debugger

- Easy high-level and assembler debugging
- Interface to all compilers
- RTOS awareness
- Interface to all hosts
- Fast download
- Display of internal and external peripherals at a logical level
- Flash programming
- Hardware breakpoints and trigger (if supported by on chip debug interface)
- Multiprocessor/multicore debugging
- Trace and trigger extension possible
- Software trace
- Virtual analyzer
- Software compatible to all TRACE32 tools

TRACE32-ICD are microprocessor development tools based on the debug and trace logic (BDM, JTAG, ETM, OCDS, NEXUS) integrated on the chip. On this basis TRACE32-ICD provides a highly cost effective debugger plus a powerful trace and run time analysis tool.

TRACE32-ICD can be connected to the host by an ethernet, USB or LPT interface.

TRACE32-ICD

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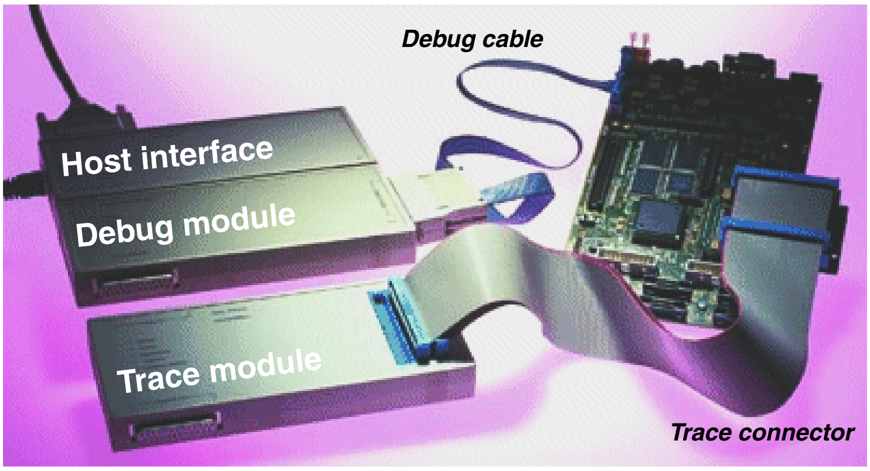
TRACE32-ICD family

TRACE32-ICD

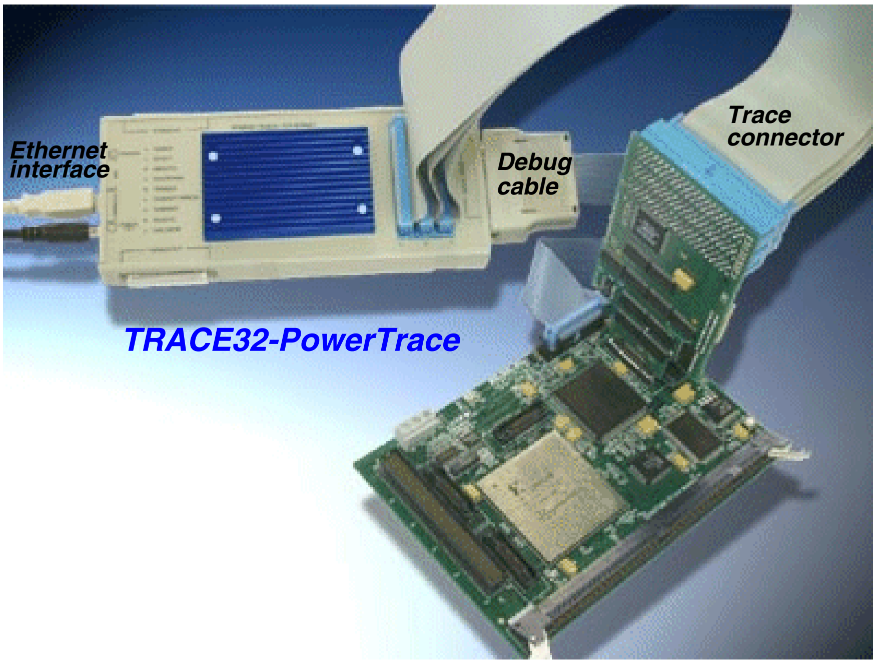
The successful In-Circuit Debugger with trace extension is available since 1995. It supports more the 15 architectures including so popular architectures like ARM and PowerPC.



TRACE32-PowerDebug/PowerTrace

TRACE32-PowerDebug/PowerTrace is a further development of the successful product TRACE32-ICD and is based on years of experience with on-chip debug and trace interfaces at Lauterbach. ***TRACE32-PowerDebug*** provides a increased system performance.

The main new features for ***TRACE32-PowerTrace*** are: increased system performance, very large trace memory, extended features for run-time measurements and performance analysis. Thus TRACE32-ICD PowerTrace fills a major gap in software quality assurance.

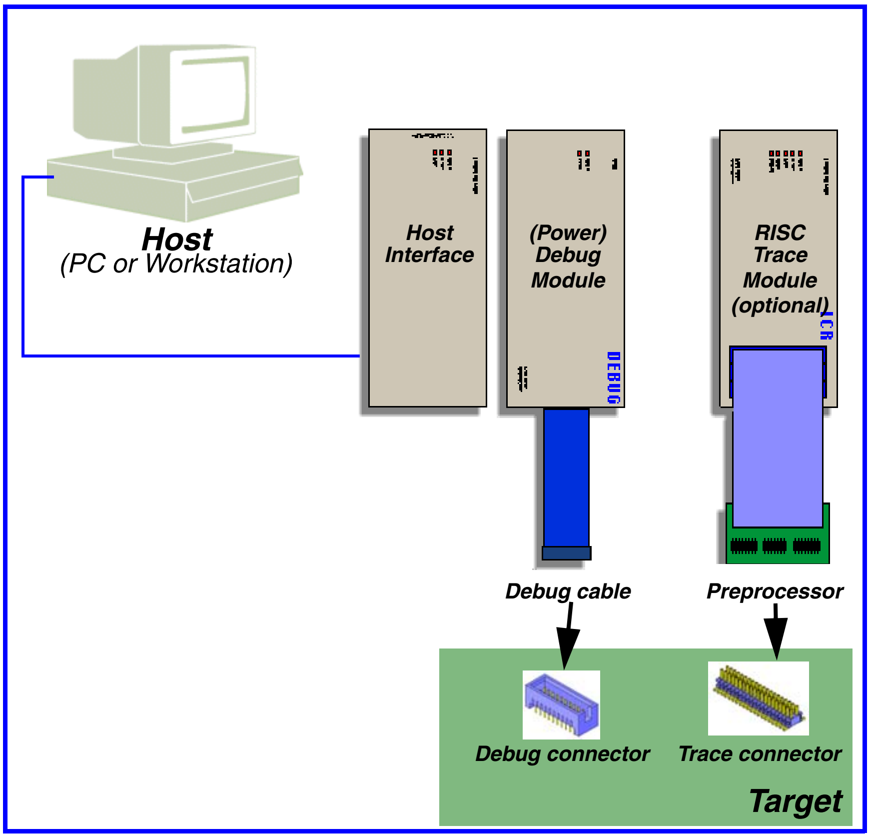


TRACE32-ICD ROM Monitor

TRACE32-ICD offers also ROM monitor solutions for all processors that don't have an on-chip debug interface. The communication between the debugger on the host and the monitor program on the target is either implemented via RS232 or via an EPROM simulator.

Hardware Concept

TRACE32-ICD



Host Interfaces

- ❑ LPT
- ❑ ISA Card
- ❑ Ethernet

(Power) Debug Module
Universal debugger hardware for all architectures.

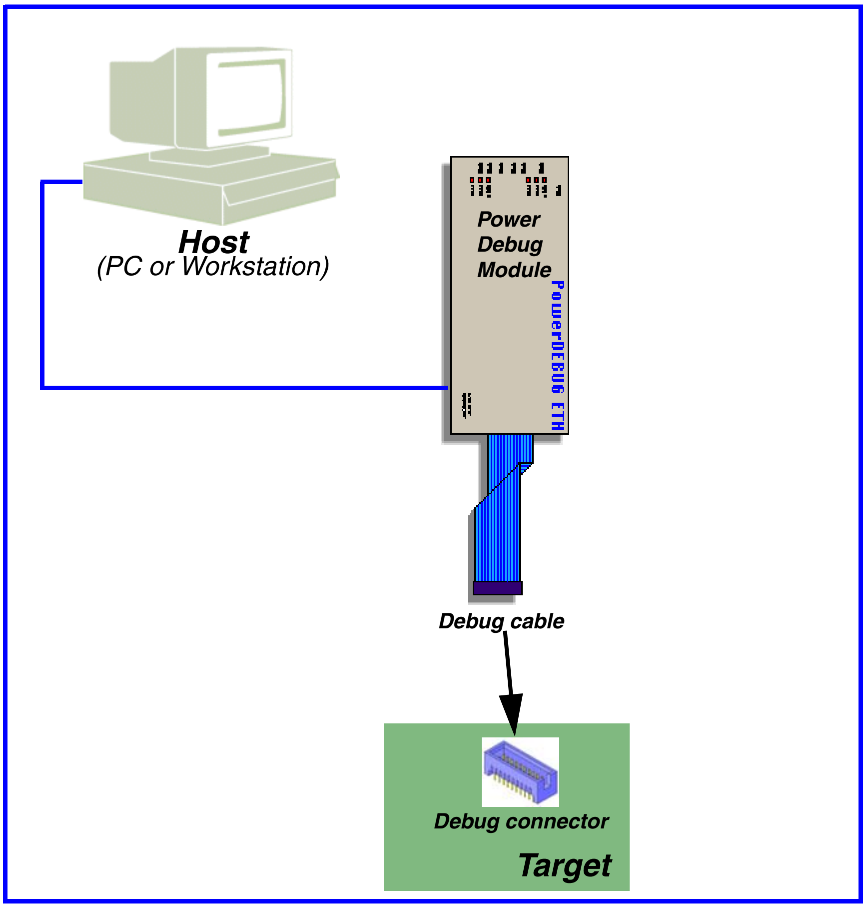
CPU specific Debug Cable

RISC Trace Module (optional)
Universal trace hardware for all architectures:

- ❑ Support for bus trace or program/data flow trace
- ❑ 64/128/256/512 KFrames trace memory
- ❑ 94 channels
- ❑ CPU specific max. speed
- ❑ 36 bit time stamp, 25 ns resolution

CPU specific Preprocessor
CPU specific preprocessor to transfer the trace data from the target to the RISC trace module.

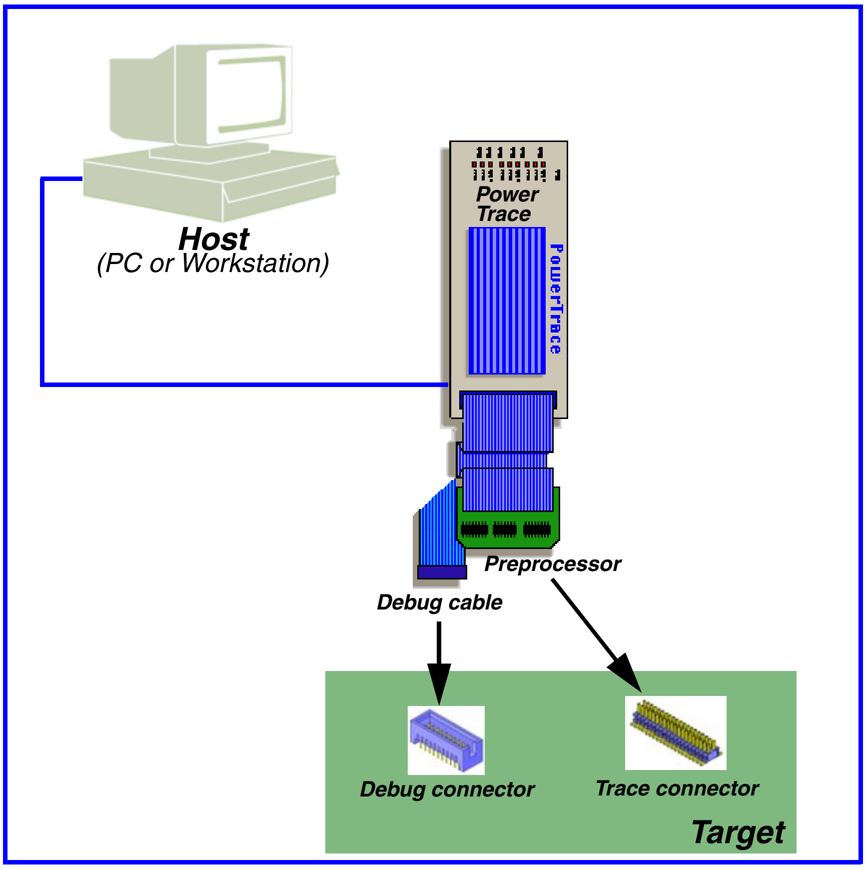
TRACE32-ICD PowerDebug



Power Debug Module
Universal debugger hardware for all architectures. Ethernet or USB interface included.

CPU specific Debug Cable

TRACE32-ICD PowerTrace



PowerTrace

- Universal debugger hardware for all architectures
- Ethernet or USB interface included
- Support for program and data flow trace
- 16MFrame trace memory
- 96 channels
- CPU specific max. speed
- 32 bit time stamp, 20ns resolution
- Non intrusive runtime and performance analysis
- Code Coverage

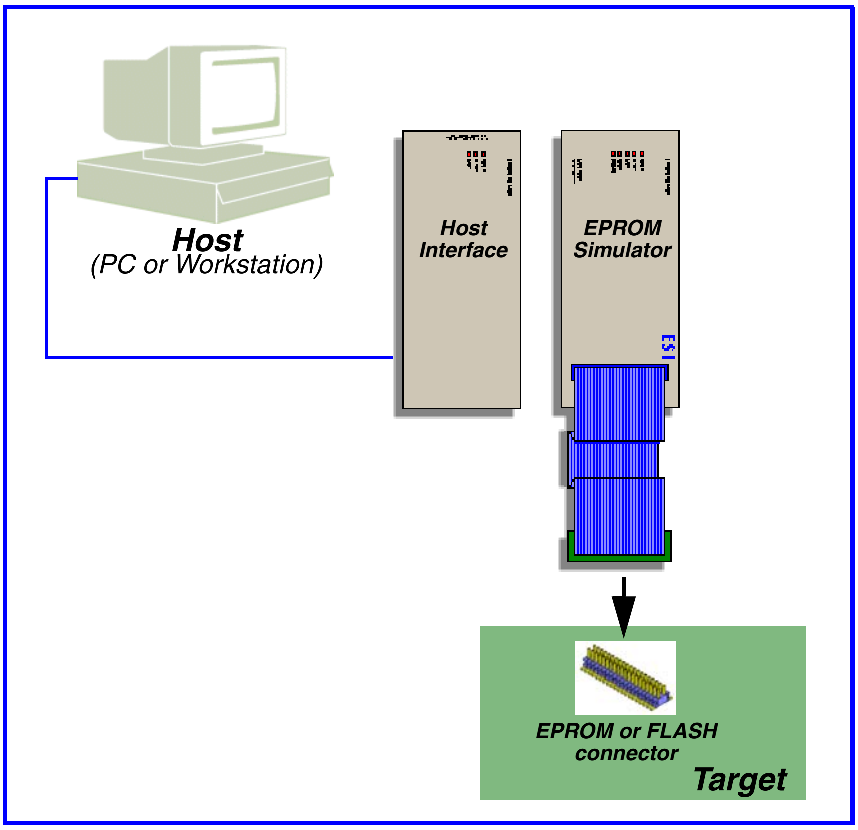
CPU specific Debug Cable

CPU specific Preprocessor
CPU specific preprocessor to transfer the trace data from the target to the trace memory of the PowerTrace unit.

TRACE32-ICD Monitor

The TRACE32-ICD Monitor is based on a ROM Monitor solution. An 8KB monitor program may be located anywhere in the address space. The monitor can be linked and loaded separately or it can be linked and loaded along with the user program. To implement the monitor, some interrupt vectors must be reserved for the monitor program use and this must be allowed for in the target software design.

The communication between the debugger on the host and the monitor program on the target is done using an EPROM simulator or via RS232.
The EPROM simulator can support two 8-bit or one 16-bit EPROM. The combination of several modules allows 32- or 64-bit configurations to be supported. During the simulation the EPROM configuration of the target system can be imitated by the software in the EPROM simulator. Using this technique paged or banked EPROM's can be simulated.



Host Interfaces

- ❏ LPT
- ❏ ISA Card
- ❏ Ethernet

EPROM Simulator

Universal EPROM Simulator

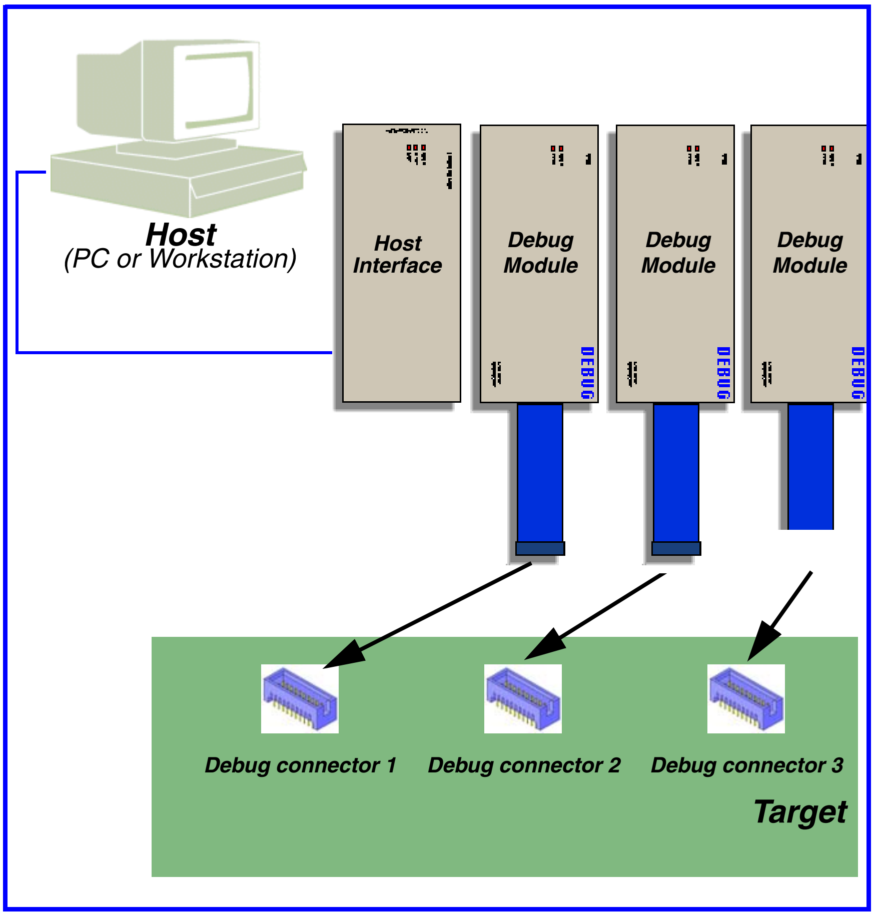
- ❏ 8/16/64MBit ERPOM Simulator
- ❏ 40 ns access time
- ❏ 5V and 3.3 V
- ❏ Connector to DIL, PLCC, SO44 and universal ESICON connector

Multiprocessor Debugging

A maximum of 4 debuggers can be connected to a host interface to configure a multiprocessor development environment. It is of course also possible to use 2 debuggers and 2 trace modules. What hardware is controlled by which TRACE32 software component is defined via a configuration file.

Start/stop synchronization

If several processors are to be started and stopped simultaneously as far as possible it is necessary to define which functions as master and which as slave in the overall configuration. The system can also be set so that all processors double as master and slave so when any processor is started all other processors are started and when any processor is stopped all others are stopped. A synchronous start can be carried out within about 10µs. Synchronous stopping, for example at a breakpoint can be implemented exactly. As a basic requirement for this, however, the debug interface of the processor used must have a trigger input and a trigger output. If this is not the case, asynchronous stopping must be implemented by software means which takes correspondingly longer.



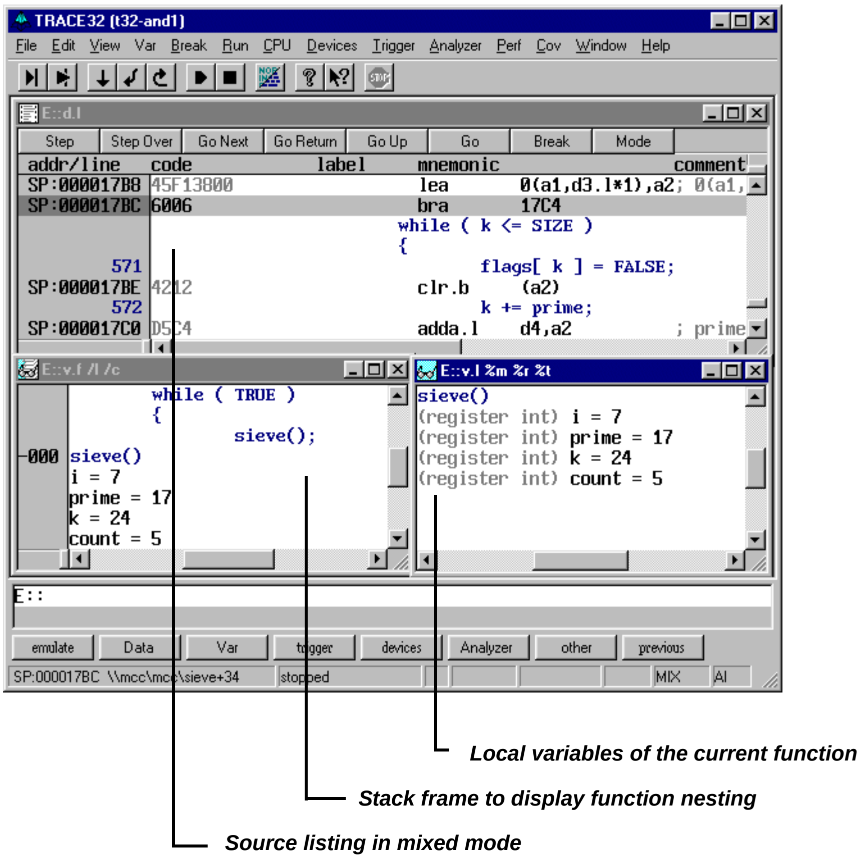
Multicore Debugging

The term multicore debugging is applied to the testing of multiple cores on a chip.
If there are several cores integrated on a chip and each core has its own debug interface the same hardware and software configuration can be used as for multiprocessor debugging.
It´s a different picture if all cores are driven via the same debug interface in order to save pins. It is possible, for example to daisy-chain several cores that run via the same debug port. This is a popular solution at present for chips with ARM cores since this arrangement is very easy to implement with the JTAG interface. In this case the debugger requires the capability to work with a specific core in the chain and to ensure that the control sequences are passed through by the other cores. In the straightforward event that the developer only wants to work with a single core the position of the core in the chain can be set by software means.

If more then one core are to be tested simultaneously several debug modules are needed as in case of multiprocessor debugging. There must be several debug connectors with the same JTAG signals on the target system. Alternatively, it is also possible to use an adapter that splits up the JTAG interface for several debuggers.
Since several debugger now use the same debug port, steps must be taken to ensure that only one debugger accesses the debug port at any time. This can be automated by the debug task on the host controlling who has exclusive access to the debug port through the use of a semaphore system.
There are of course other configuration options for multiple cores in a chip apart from daisy chaining. For more information on this topic contact our technical support.

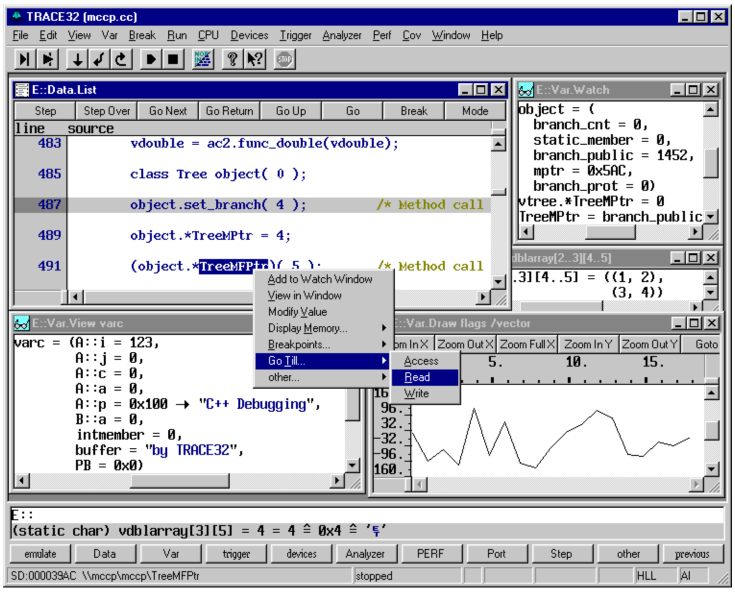
Software Concept Debugger

Symbolic Debugging



A hierarchical symbol database enables structured symbolic debugging. Symbol names can be up to 255 significant characters long and can be used to show single program addresses, module names and memory classes. The disassembler can use the symbols for labels and/or operands. Demangling for C++ signatures is supported.

High-Level Language Debugging



TRACE32 can directly load the output of all standard compilers for C, C++, JAVA, Pascal, Modula2, PEARL and ADA from most compiler vendors. Program display and debugging can be done in assembler, high-level or in a mixture of both. It is possible to construct both assembler and high-level windows on the screen simultaneously. All variable types specific to the high-level language can be displayed and modified. Addresses can be absolute, relative or line number based.

Debugging

The debugger uses the following breakpoint implementations to stop the program execution at a certain instruction:

- ❑ unlimited number of software breakpoints for code in RAM
- ❑ a limited number of so-called onchip breakpoints for code in ROM/FLASH

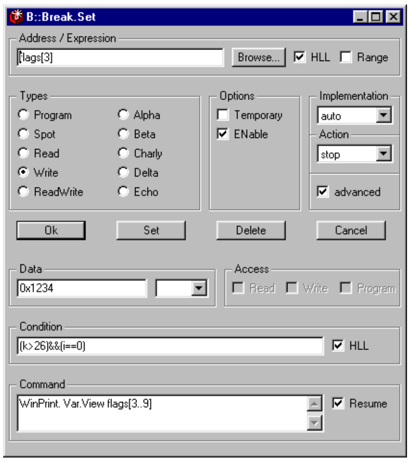
The onchip breakpoints can also be used to stop the program execution after a read/write access to a specific memory address.
The number of available onchip breakpoints depends on the resources provides by the CPU used.

Advanced breakpoints

TRACE32-ICD provides also a simple way to set complex break conditions:

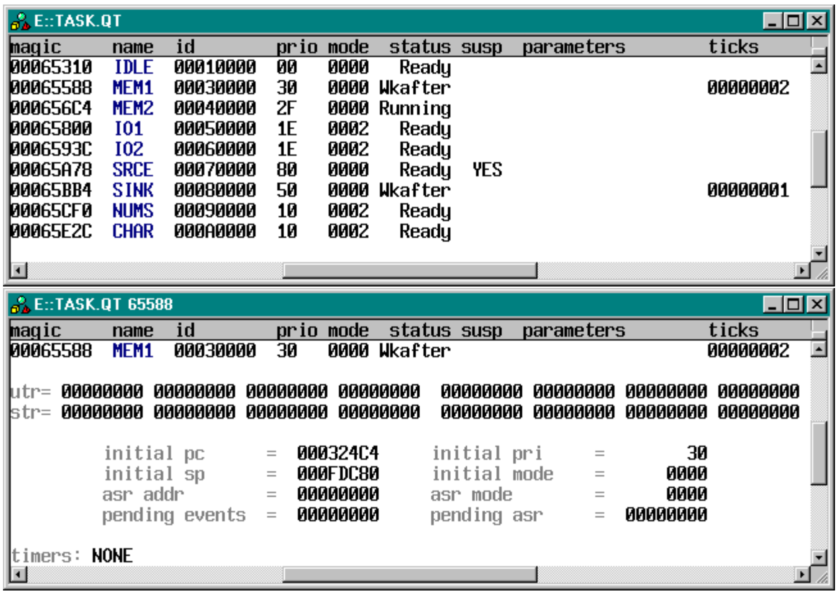
- Setting of breakpoints to the reading and writing of specific data values
- Linking the breakpoint with a condition
- Linking the breakpoint with commands that are executed whenever the breakpoint is reached
- Spot breakpoints on data accesses

A combination of all 4 new features is also possible.



RTOS Awareness

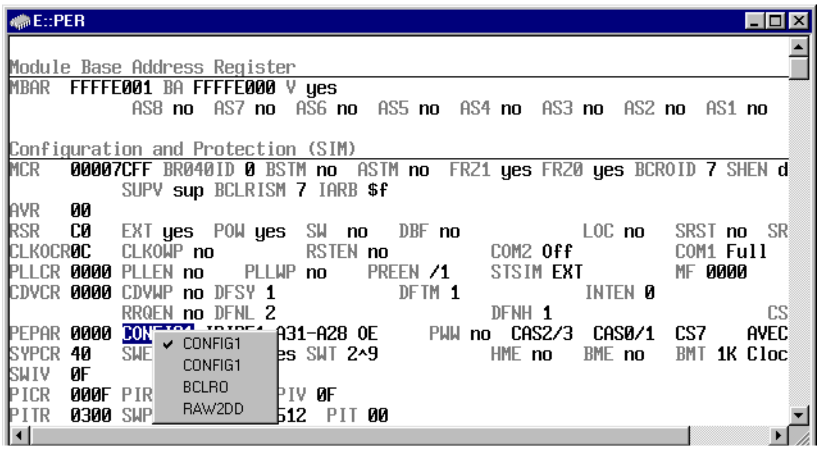
The In-Circuit Debuggers provide display functions, closely mirroring the command set of the integral debugger of the RTOS. The system resources e.g. tasks, objects, partitions, queues, regions and semaphores can be displayed. These functions are also available if the integral debugger is not linked to the software.



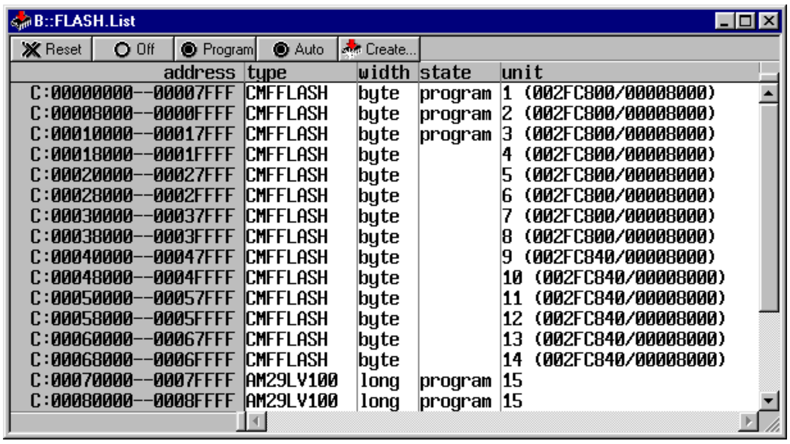
Task list window and detailed window of one specific task

Peripherals

- ❑ Display of onchip peripherals
- ❑ User definable display of the onchip peripherals
- ❑ Definition is done interactive supported by softkeys
- ❑ Pull down menues for settings
- ❑ Additional description for each field
- ❑



Flash Programming



TRACE32 support the programming of external flash memory as well as the programming of internal flash memory of microcontrollers. The programming can be controlled by the debugger or by a routine in the target system.

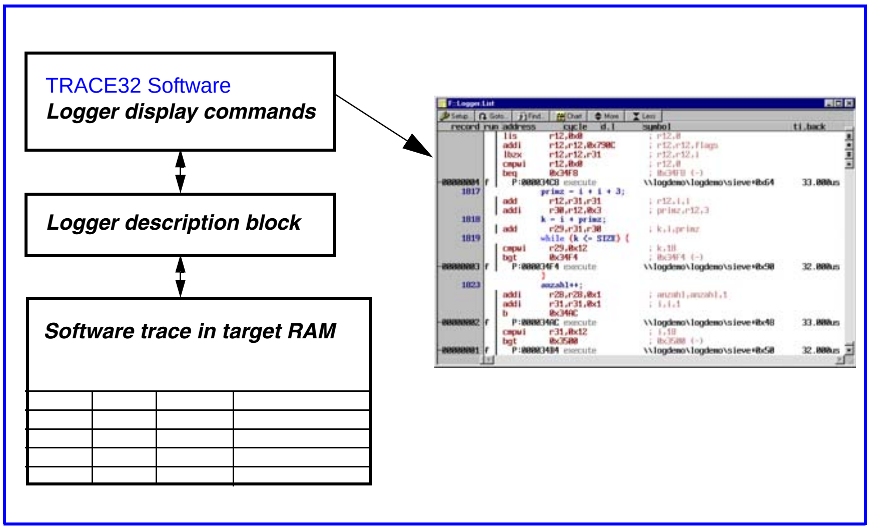
Software Trace

If your TRACE32-ICD is not equipped with a trace extension you can use the software trace feature to sample data and program information.

Here instead of the real trace memory an array structure on the target is used to store the trace data. Entries to this array can be made by instrumenting the target program.

The same trace display commands can be used for the software trace and the real trace memory. This includes performance measurements and time charting. A typical use of the software trace is the trace and analysis of task switches.

A program flow trace is available for architectures which provide a ´branch trace´ capability, like all PowerPC families and the SuperH SH4.



Performance Analysis

TRACE32-ICD offers a long-term performance analysis. For example, to determine which function or module uses the greatest proportion of the total run time the current program counter is recorded periodically and evalutated statistically.

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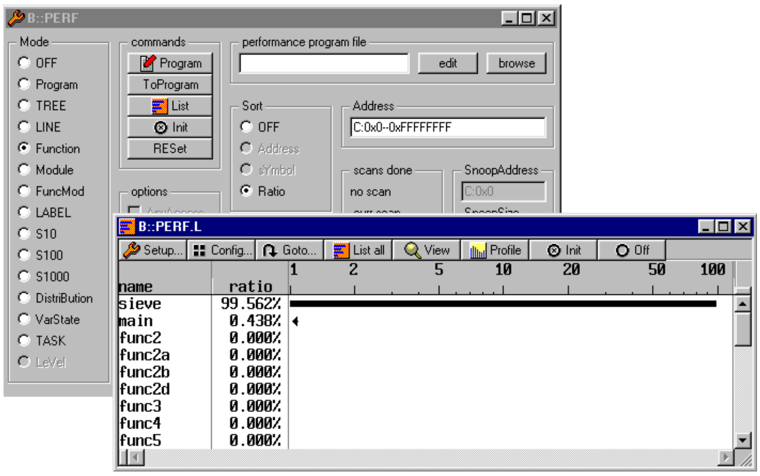
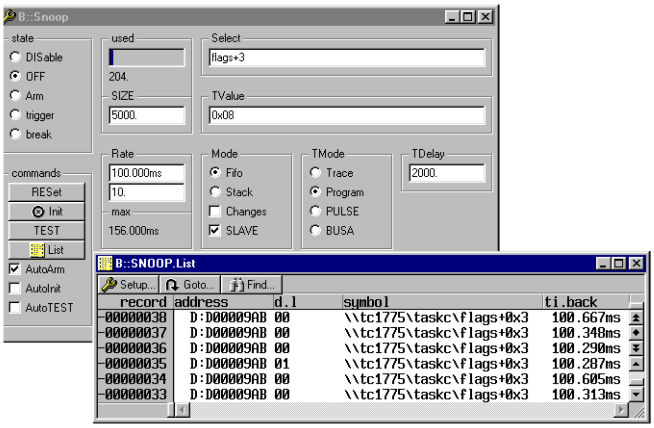


Virtual Analyzer

TRACE32-ICD provides the feature to monitor changes in selected data over a period of time. As a basic requirement for this feature, the debug interface of the CPU used must support to read the target memory while the program is running.

To monitor selected data the virtual analyzer reads out the corresponding memory cells in a fixed time pattern during the program run and transfers their contents to its virtual trace memory. Since the virtual trace is pure software it can be of any size.



Powerful Script Language

The TRACE32 batch language PRACTICE support automatic test, automatic system configurations and the construction of command macros to expedite our development cycle.

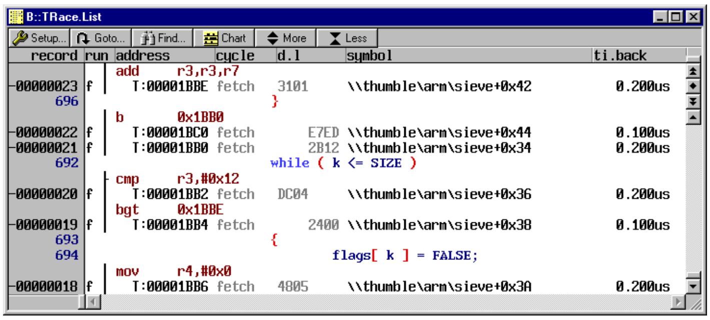
GUI Customization

The TRACE32 user interface is open and allows to adapt menus, buttons and dialogue boxes intuitively to the customers need.

Software Concept Trace

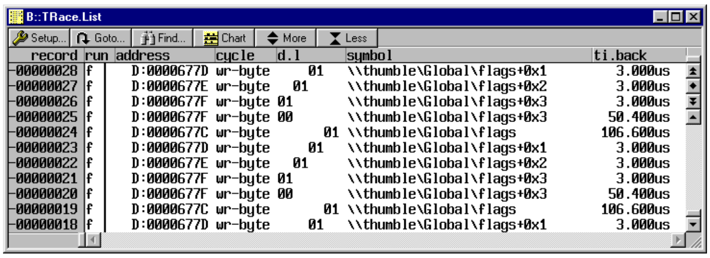
Bus Trace

The trace extension of TRACE32-ICD works as a bus trace for some CPUs. For a bus trace the address and data bus and certain state lines are recorded for every bus cycle. As a result the complete information about the program and data flow is available.



Selective Tracing

The trace extension for TRACE32-ICD provides some basic features for selective tracing.

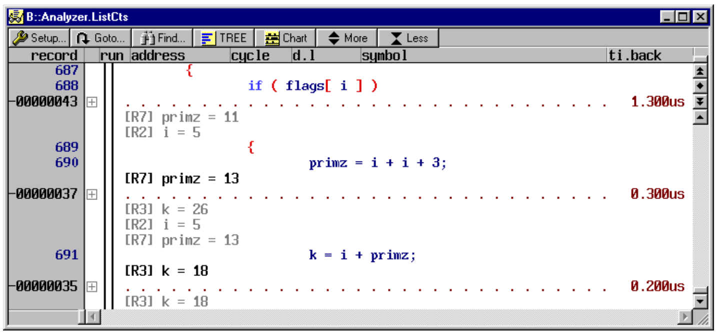


HLL Trace

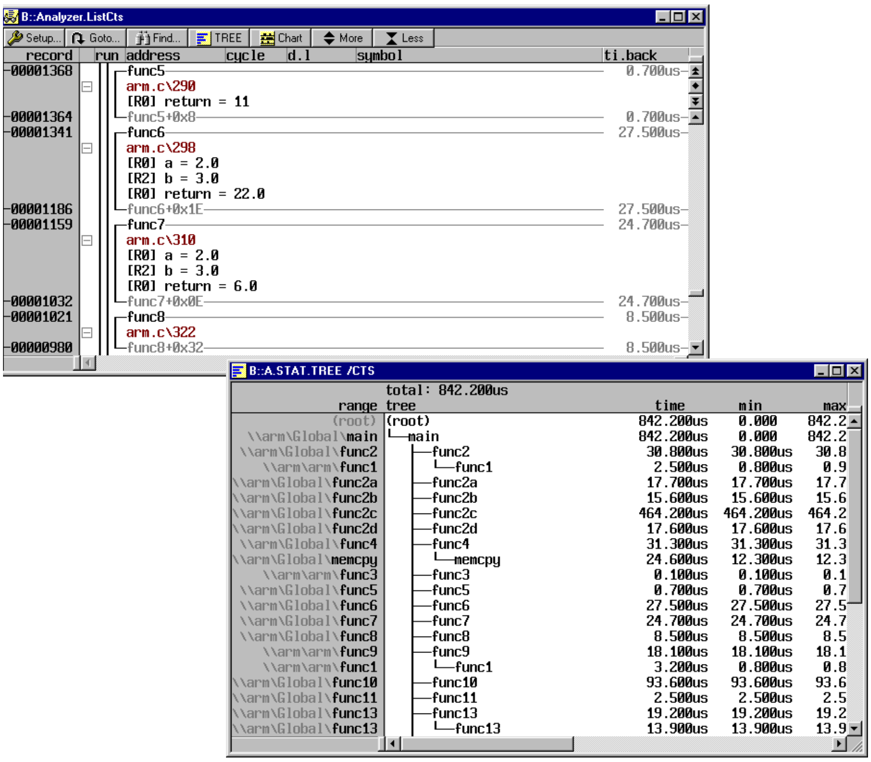
The context tracking system (CTS) makes it possible to show also register and stack variables in the trace display.

For each high-level language step sampled in the trace buffer, the developer receives:

- the current values of the variable used
- the result of the program step
- the exact time needed



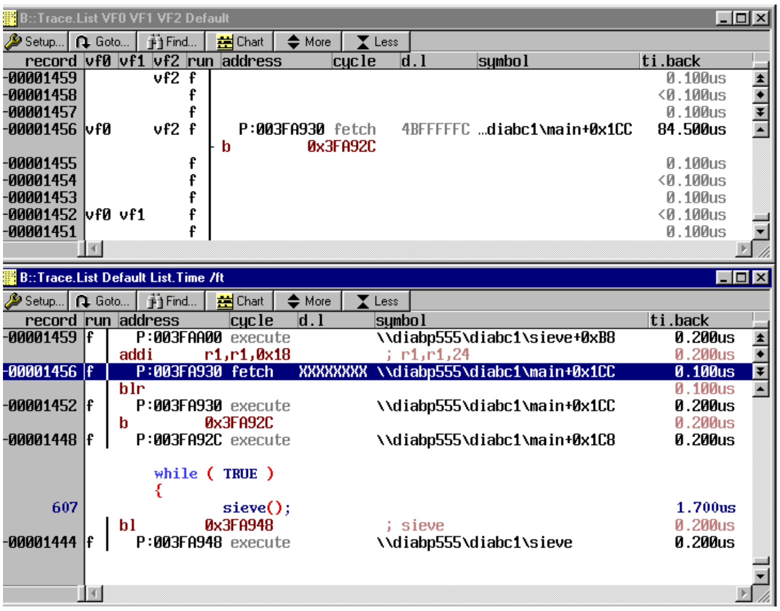
CTS can also be used for a detailed function nesting analysis over the whole trace memory. Function parameters, return values, and function run time are indicated for each function. This analysis can also be carried out graphically in the form of a call tree.



Program Flow Trace

The trace extension of TRACE32-ICD works as a program flow trace for most CPUs.
Due to high speeds most CPUs don't provide full visibility of the internal program and data flow. They are equipped with a so-called trace port (special pins of the CPU). Through this trace port reduced information about the internal program run are output. This reduced information comprises program status information, branch destination addresses of direct/indirect branches and on some CPUs reduced data flow information.
TRACE32-ICD sample this information for each clock and processes the data to offer the developer full information about the program/data flow.
The reduced data submit to little information to provide features for selective tracing.

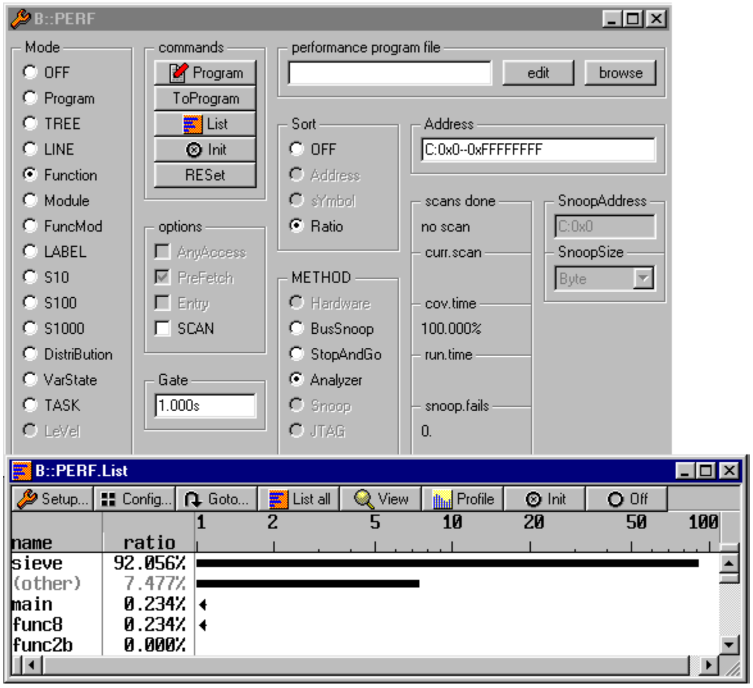
Sampled information



Reconstructed program and data flow

Trace based Performance Analysis

The performance measurement used by TRACE32-ICD is a statistical process. To determine for example which function or which module uses the greatest proportion of the total runtime the recording into the trace memory is stopped briefly to determine the current program counter contents. This measurement has absolutely no influence on the real-time behaviour.



LAUTERBACH
DEVELOPMENT TOOLS

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