

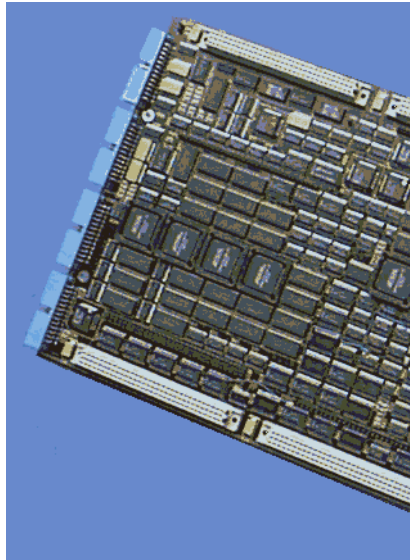
State and Performance Analyzer

- 120 Channel Trace
- High-Level Trigger Unit
- 25 ns Time Stamp
- Master-Slave Trigger
- Selective Trace
- Statistic Display
- Timing Display
- Performance Analyzer
- Coverage Analysis

The TRACE Analyzer HA120 is designed as a high-speed state analyzer for CPU cycle times up to 50ns . Because of recent and very fast integrated circuits, the analyzer offers a 32 Kbyte trace memory with a system synchronized time stamp unit, with powerful and complex trigger capabilities, and an independent performance analyzer on only one board. All important line of the CPU are automatically connected to the analyzer.

Universal input and output lines for trigger and stimulation are available via additional input and output pods.

State Analyzer HA120



120 Channel Trace

The HA120 samples 120 bit per record. For 32 bit processors, additional trace buffer are located on the base modules. Up to 344 bit per record can therefore be controlled by the analyzer.

- 24 bit address
- 4 bit address range
- 16 bit data
- 8 bit state signals
- 4 bit bank access signals
- 24 bit universal channels
- 3 bit markers
- 3 bit 8 trigger levels
- 16 bit external trigger inputs
- 1 bit DMA access
- 4 bit task no.
- 8 bit reserved
- 5 bit internal

High-Speed, down to 50ns Cycle Time

If necessary , CPU cycles up to 50 ns can be recorded. Also complex trigger input and output functions

can be performed in 50 ns without touching real time program execution.

Large Trace Depth (32KFrames)

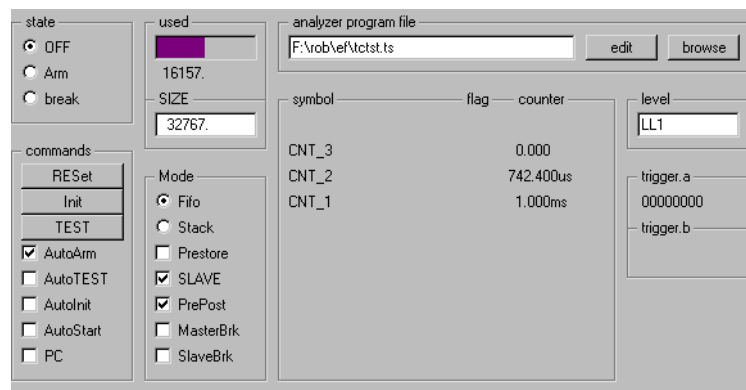
The trace depth reaches 32 KFrames . This is much more than necessary , because of the flexible

trigger unit, which allows exactly to specify the contents of the trace memory.

Hypertrace with up to 4 MFrames

For statistics and function tree purposes, an additional board can be mounted on the HA120, which extends the trace depth up to 4 MFrames.

Operation Modes

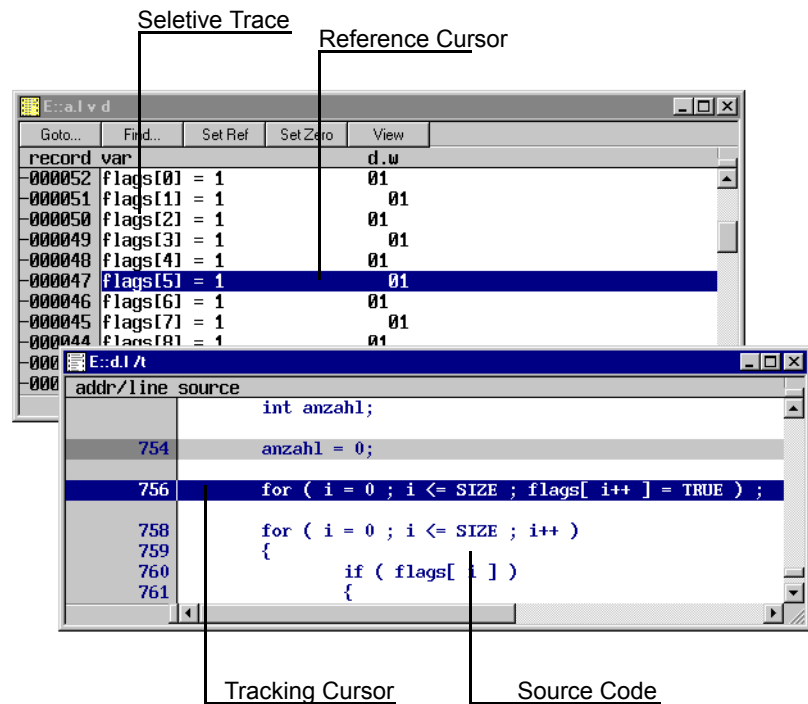


- FIFO mode
 - records all until user program has been stopped.
- STACK mode
 - records from program start until the trace memory is full.

PRESTORE Function

In the PRESTORE mode, the analyzer samples always an additional previous Opfetch cycle forced by

hardware, if only data transfers should be sampled selected by the trigger unit.



Internal Expansion Capability

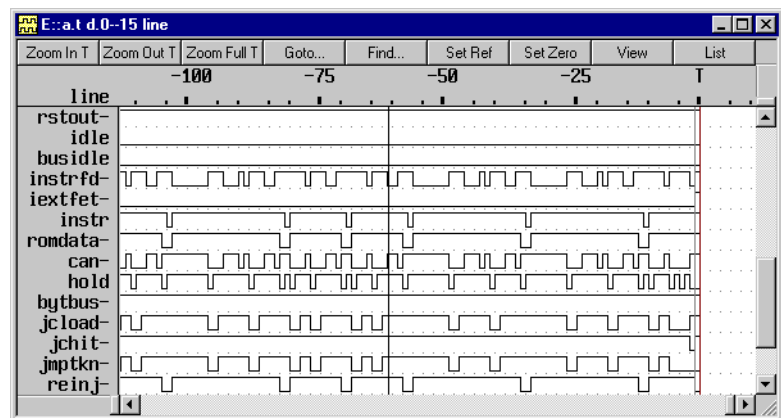
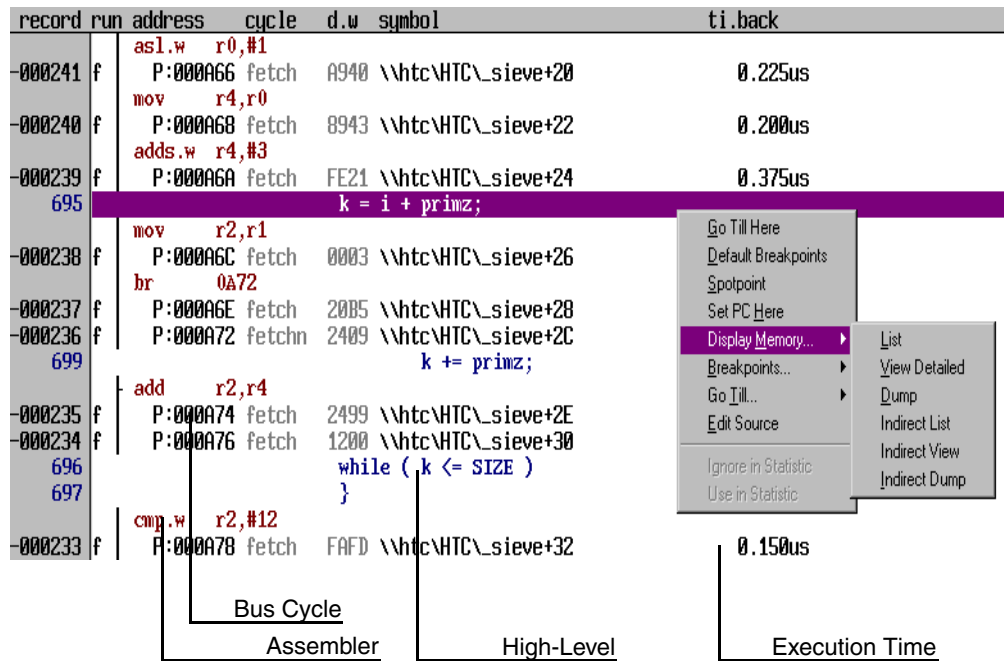
For emulator modules which need more trace capacity, the necessary extra bits are built into the emulator

module itself (e.g. 64 additional channels with the trace board on microcontroller emulation heads).

Various Trace Memory Display

- List
- Timing
- Chart
- Recordwise
- Assembler mnemonic
- Hex, binary, ASCII, etc.
- High Level Language
- Mixed language

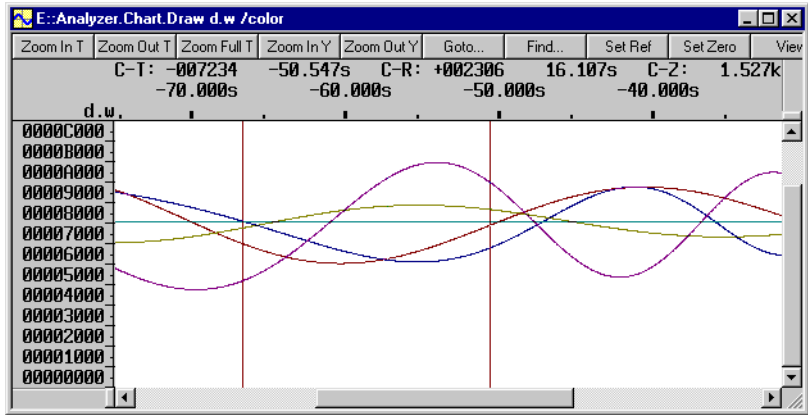
Program source tracking



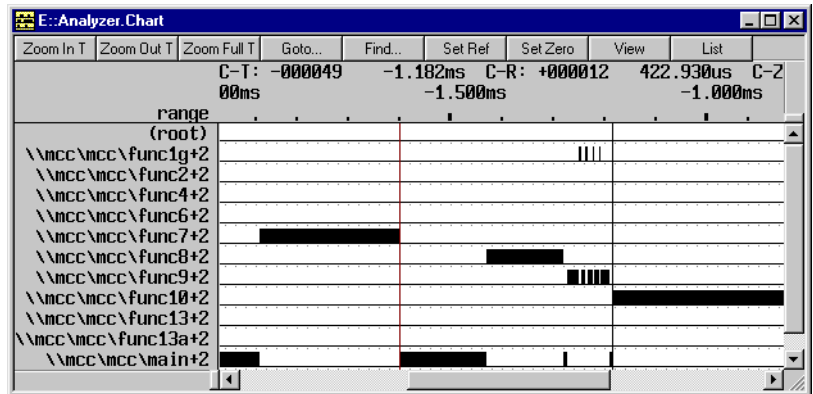
Cursor

Ref. Cursor

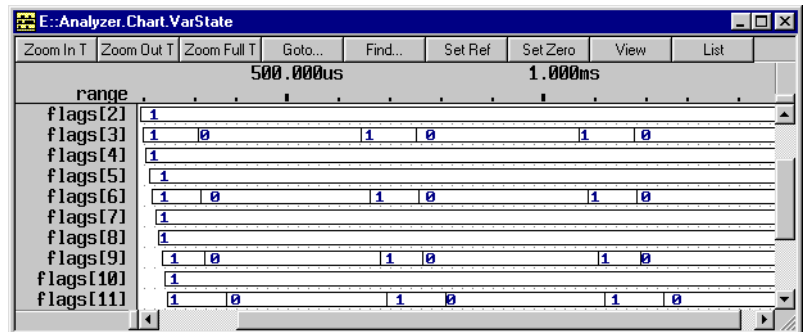
Trigger



Graphical Display



Execution Time Chart

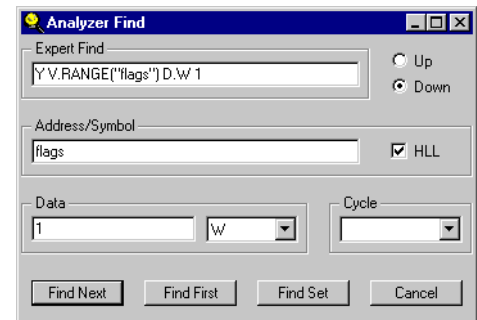


Variable Time Chart

Powerful Trace Memory Manager

- Save memory
- Load memory
- Print memory
- Compare memory
- Find specific entry
- Goto record
- Time and record number evaluation.
- Referenz pointer

- User defined display



Trigger Unit

Analyzer Trigger Unit with 8 Levels

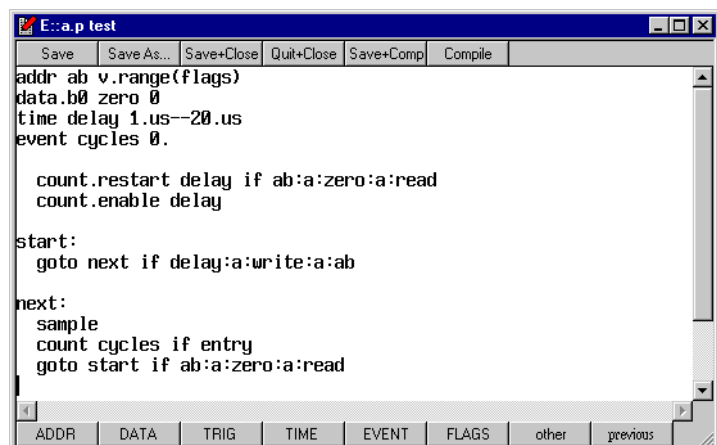
The level structure of the trigger unit allows very flexible trigger combinations and sequences in consecutive and nonconsecutive order. Each level has the same priority and the same

capabilities. A trigger program defines, under which circumstances a level can be reached or left, and therefore which trigger conditions or operations are the current or the next.

Analyzer Programming via a special Window

The programming of this complex trigger unit is done in an assembler like language for maximum flexibility. Using this language, the programming of very

complex trigger sequences or operations can be defined. For simple demands, a pull down menu improves the programming for beginners.



```
E::a.p test
Save Save As... Save+Close Quit+Close Save+Comp Compile
addr ab v.range(flags)
data.b0 zero 0
time delay 1.us--20.us
event cycles 0.

count.restart delay if ab:a:zero:a:read
count.enable delay

start:
goto next if delay:a:write:a:ab

next:
sample
count cycles if entry
goto start if ab:a:zero:a:read

ADDR DATA TRIG TIME EVENT FLAGS other previous
```


Fast Programming by Menu

Symbolic Operations for Analyzer Programming

All output operators and input variables can be entered in symbolic form. The target program symbols can also be used.

Trigger Sources

- Up to 6 address ranges
- Up to 6 data events (mask, range, ASCII, hex, binary)
- Up to 16 external trigger events
- CPU state (MEM READ, IO WRITE, INTA, ...)
- Counter outputs

External Trigger Inputs

- 2 inputs with 8 channels
- 2 trigger qualifiers for each trigger level
- Static levels of the trigger inputs can be read at any time
- Free format definition of external trigger events

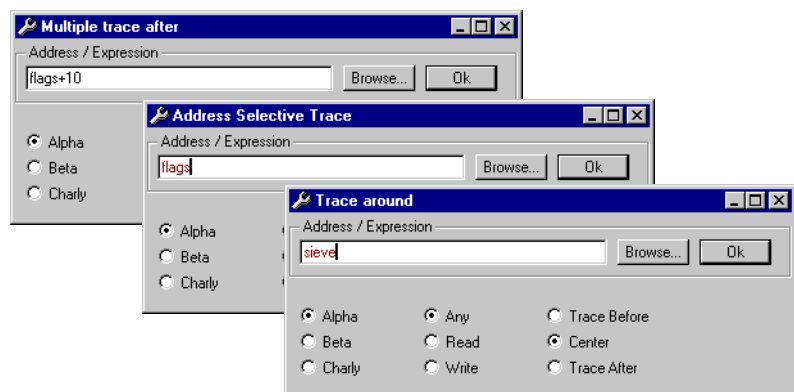
Trigger Output Operations

- | | |
|---|--------------------------------------|
| <input type="checkbox"/> Count.Restart | <input type="checkbox"/> Break |
| <input type="checkbox"/> Count.Enable | <input type="checkbox"/> Bus.Trigger |
| <input type="checkbox"/> Sample.Enable | <input type="checkbox"/> Spot |
| <input type="checkbox"/> Trigger.Emulator | <input type="checkbox"/> GOTO level |
| <input type="checkbox"/> Trigger.Exception | <input type="checkbox"/> Mark record |
| <input type="checkbox"/> Out (Target Stimulation) | |

Free Format Definition of Data, Address and Trigger Events

- | | |
|--|---|
| <input type="checkbox"/> Hex and hex masks | <input type="checkbox"/> ASCII character and string |
| <input type="checkbox"/> Binary and binary masks | <input type="checkbox"/> Data ranges |

Wizards for Standard Trigger Problems



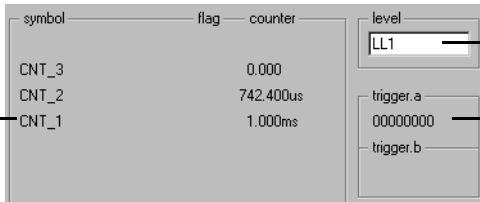
Time and Event Measurements with up to 3 Counters

There are 3 40 bit counters available for event measurement or event triggering. All counters are re-triggerable and can be evaluated as a part of an expression in the trigger sequences. Each counter can be programmed as a timer for timing measurements or an event counter.

- | | |
|---|--|
| <input type="checkbox"/> Event count 1 to 1.1E+12 | <input type="checkbox"/> Time 100ns to 1.3 days |
| <input type="checkbox"/> Cycles 1 to 1.1E+12 | <input type="checkbox"/> Retriggerable |
| | <input type="checkbox"/> Selective release |
| | <input type="checkbox"/> Trigger event when counter is zero |
| | <input type="checkbox"/> Definition of time and event windows |
| | <input type="checkbox"/> All Counters can be read 'on the fly' |

Trigger Monitor

A display of the counter values, the trigger values, the trigger levels and the trigger flags is available in the trigger monitor window.



The screenshot shows a window with a table of counter values and a panel for trigger levels. The table has columns for 'symbol', 'flag', and 'counter'. The counter values are 0.000 for CNT_3, 742.400us for CNT_2, and 1.000ms for CNT_1. The trigger level panel shows 'LL1' as the trigger level and '00000000' as the input level for trigger.a.

symbol	flag	counter
CNT_3		0.000
CNT_2		742.400us
CNT_1		1.000ms

level: LL1 (Trigger level)

trigger.a: 00000000 (Input level)

trigger.b:

Statistic Analyzer

Time Stamp

The Time Stamp Unit tags each trace record with a time value. These values are absolute and synchronized with all the other time values within the TRACE32 system.

Recording depth max. 32K

48 Bit time stamp recording

Resolution 25

Maximum measuring time 1.3 days

Function Analysis

Min. and max. time

Include and exclude time

Passes

Link Analysis

Callers

Calls

Min. and max. times

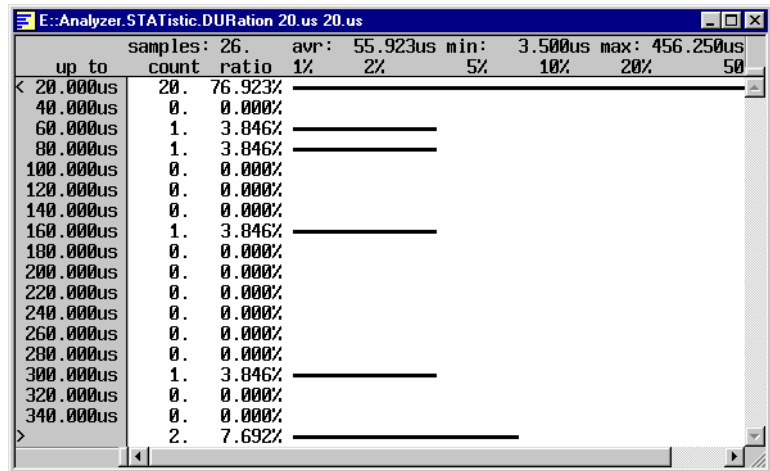
The screenshot shows a window titled "E::Analyzer.STATistic.TREE tree time count avr". The content is a tree view of function call statistics. The root node is "(root)" with a total time of 2.886ms. Below it is a tree structure of function calls, each with its own time, count, and average time.

tree	time	count	avr
(root)	2.886ms	1. (-2)	2.886ms
└─main+2	2.885ms	1. (-1)	2.885ms
└─func2+2	211.750us	1.	211.750us
└─func1g+2	7.000us	2.	3.500us
└─func4+2	64.000us	1.	64.000us
└─func6+2	386.000us	1.	386.000us
└─func7+2	281.750us	1.	281.750us
└─func8+2	152.500us	1.	152.500us
└─func9+2	85.250us	1.	85.250us
└─func1g+2	14.000us	4.	3.500us
└─func10+2	456.250us	1.	456.250us
└─func13+2	227.250us	1.	227.250us
└─func13+2	166.250us	1.	166.250us
└─func13+2	104.750us	1.	104.750us
└─func13+2	43.500us	1.	43.500us
└─func13a+2	455.250us	1.	455.250us

Duration

Execution time

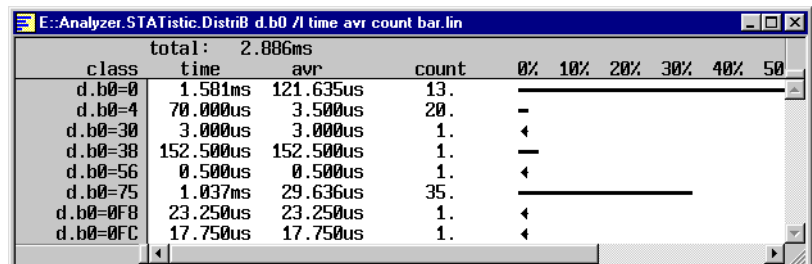
- Response time



Distance

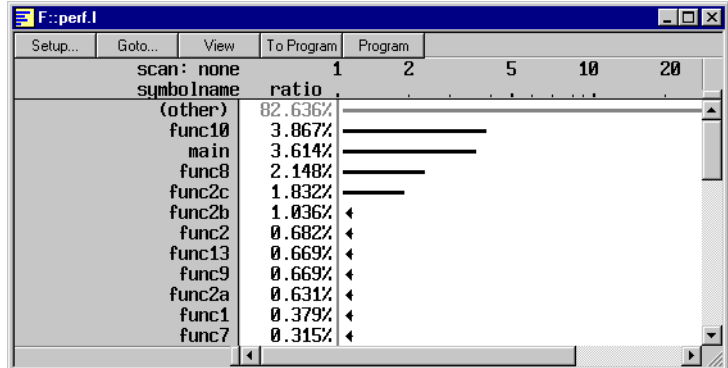
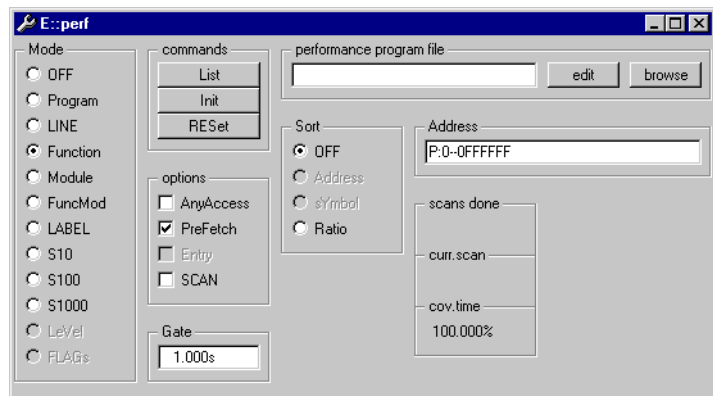
- Time between samples

Distribution



Performance Analyzer

- Resolution
 - 1 us
 - Reatime Measurement
- Performance Analyzer Modes
 - Program address
 - Access
- Performance Address Ranges
 - Modules
 - Functions
 - Address ranges
 - Trigger Level
 - Flags



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Detailed Order Information

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