



FIRE Emulator for ST10

C165
 C167
 C167C
 C167CR
 C167CS
 C167CW
 C167SR
 ST10F163
 ST10F167
 ST10F168
 ST10F169
 ST10F251
 ST10F251M
 ST10F252
 ST10F252M
 ST10F269
 ST10F271
 ST10F271B
 ST10F271M
 ST10F272
 ST10F272B
 ST10F272M
 ST10F273
 ST10F273M
 ST10F275
 ST10F276
 ST10F280
 ST10F293
 ST10F296

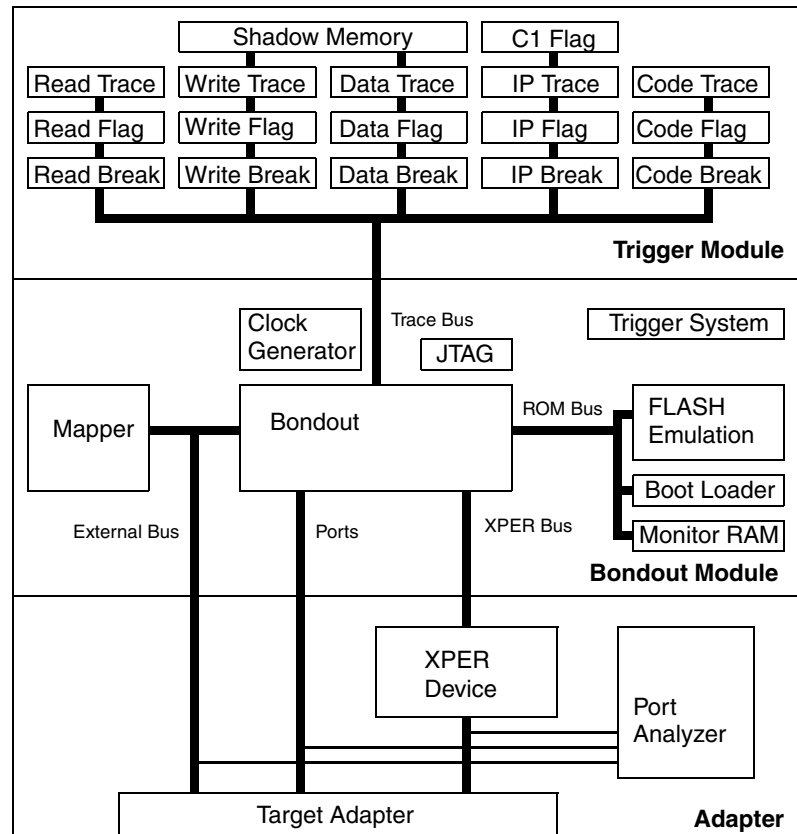
- Full support for ST10 family
- Full support for KEIL, TASKING, COSMIC and GNU compilers
- 50 MHz no-wait-state operation
- Dual-port access for ROM and external bus
- Dual-port access for XRAM
- Shadow-RAM for IRAM and XRAM
- FLASH Programming Support
- Trace on internal and local variables
- Selective trace on registers, peripherals and local variables
- Trigger on internal register access, bit, byte, and word variables
- Trace on external and BONDOUT busses, bus and clock cycle trace
- Clip-Over, Solder-On and YAMAICHI adapters

The FIRE-ST10 emulator module supports the whole ST10 family. All features of the BONDOUT chips are supported, trigger and selective trace is possible on internal addresses and data, on registers and on peripheral accesses. 128 extra trace channels are used to trace all BONDOUT signals. The ROM and FLASH memory is emulated by an extra emulation system with separate

breakpoints and execution flags for code coverage. The emulator can simulate bootstrap sequences and FLASH operation.

Features

Basics of Operation



The TRACE32-FIRE-ST10 supports all features provided by the bondout chip. The bondout chip has 4 bus systems:

- External bus
- ROM emulation bus
- XPER bus
- Bondout trace bus

The **ROM emulation bus** emulates together with the 512K emulation RAM on the base module the on-chip ROM or FLASH memory.

The **XPER bus** is needed for the emulation of CAN, ASC1 or IIC derivatives. Since the bondout chip does not contain any peripherals, there is a socket on the emulation module to add the specific CAN derivative. For the operation, the core of the derivative is disabled and the bondout CPU uses the XPER bus to emulate the peripherals.

The **Bondout trace bus** provides all signals for tracing on internal operations. Since most of the transfers are made between the internal RAM, registers and internal peripherals, these busses are a big help for analyzing the application's behaviour.

Operating Modes

The Emulator can work in stand-alone mode with internal clock or in active mode with internal or the target clock. On power-down of the target system the emulator tristates its output buffers and isolates its internal emulation circuits.

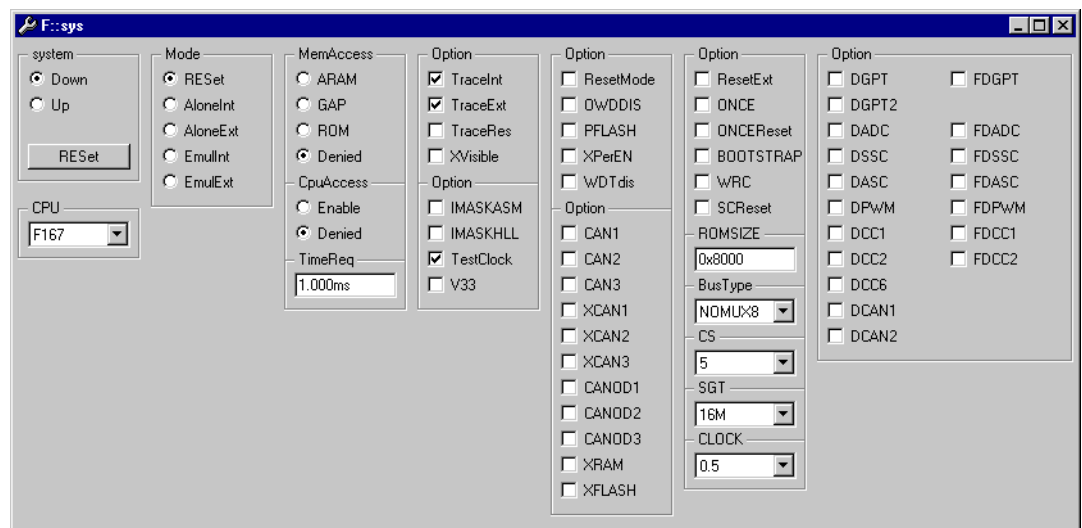
The operation modes are as follows:

- Reset
- Alone Internal
- Alone External
- Emulation Internal
- Emulation External

Clock

- Operation with external or internal Clock
- 1..150 MHz internal clock

Dual-Port Access



All TRACE32 memories are dual-ported. The dual-port access makes it possible to display and modify the contents of the overlay memory, to set or delete breakpoints or use the flag memory while the application is running in real-time.

The dual-port access on the ROM bus (on-chip ROM and FLASH emulation) is always possible. There are no limitations on breakpoint and flag usage.

The external bus has 3 modes for dual-port access

- ARAM
- GAP
- ROM
- CPU

The **GAP modes** need extra time, as the dual-port cycle is inserted while the CPU bus is set to idle. This means that less than 1% of the performance is lost by dualport cycle. In **ARAM** mode dualport cycles are done in interleave mode to the ARAM dualported RAM module.

Dualport in **ROM** is possible at any time without extra wait states. In **CPU** mode the injected access is used. This mode allows access to all type of memories including memories on target systems.

JTAG Support

A hardware based JTAG controller drives the TAP controller with 20MHz. Downloads by JTAG can be done with 300 kBytes/sec.

ROM Emulation

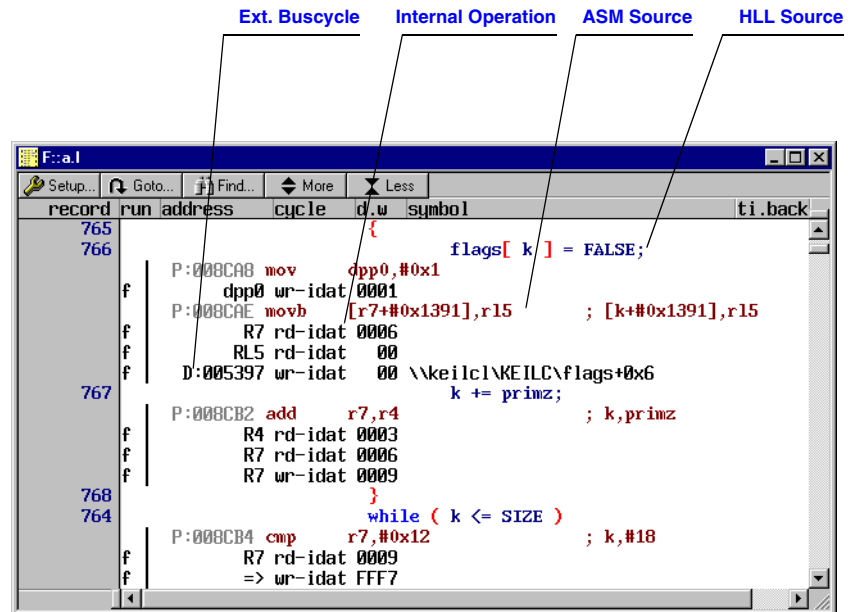
The ROM emulation circuits build a separate emulator system to emulate all on-chip FLASH or ROM based applications.

- 512K ROM emulation memory
 - FLASH and ROM emulation
- 64K Bootloader RAM
 - Bootstrap loader support

Bondout Trace

128 additional trace channels are supported by TRACE32-FIRE-ST10 to trace all signals delivered by the bond-out busses. The trace can display internal operations like register to internal memory, peripheral to registers, etc. Stack operations cannot be displayed because there is no information on the bus.

The bondout trigger and trace system uses a complex de-pipeline mechanism to make trace and trigger settings easy for the user. Operand or instruction addresses can be combined very easy for triggering on local variables.



Trace Channels

The bondout trace samples the 128 channels for BONDOUT busses. These channels provide the following information:

- Instruction execution address
- Operand read address
- Operand write address
- Operand data
- Control lines
- Instruction code

Trace Operation

The trace can work on the external bus, the internal bus or on both busses (mixed trace) to sample:

- Internal CPU cycles (BONDOUT only)
- External bus cycles
- Mixed trace

Bondout Trace

The bondout trigger and trace system uses a complex de-pipeline mechanism to make trace and trigger settings easy for the user. Operand or instruction addresses can be combined very easy for triggering on local variables.

Bondout Trigger System

The bondout trigger system works on the code flow and the other bondout signals to qualify states for internal trigger accesses. Trigger points can be set on operation results, on 24 bit addresses. All trigger points can be qualified by program segments like functions, program lines, etc.

The following trigger points are available:

- 4 1 Mbyte areas for operand read breakpoints with data qualifiers (Results of operation)
- 4 1 Mbyte areas for operand write breakpoints with data qualifiers (Results of operation)
- 2 separate data breakpoints (value, range or pattern)
- 8 1 MByte areas for instructions breakpoints (hardware breaks)

Every breakpoint can be used to stop emulation or as a input event for the trigger sequencer of the analyzer.

Data Coverage

For the read and write operations 2 flags systems are available. All systems have single byte resolution.

- 2 Read Flag Areas with 1 (4) MByte each.
- 2 Write Flag Areas with 1 (4) MByte each.

Code Coverage

The code coverage system allows 100% true code coverage and 100% C1 analysis. Prefetches are ignored.

- 2 Ranges with 1 (4) Mbyte each
- C1 Analysis

coverage	addr/line	code	label	mnemonic	comment
partial	452	int func11(x)			/* multiple retur
		int x;			
		{			
partial	455	switch (x)			
ok	P:008724	F048	func11:	mov	r4,r8 ; r4,x
ok	P:008726	2842		sub	r4,#0x2
not taken	P:008728	2D0E		jmpr	cc_eq,0x8746
ok	P:00872A	2841		sub	r4,#0x1
not taken	P:00872C	2D0F		jmpr	cc_eq,0x874C
ok	P:00872E	2841		sub	r4,#0x1
not taken	P:008730	2D10		jmpr	cc_eq,0x8752
ok	P:008732	2842		sub	r4,#0x2
not taken	P:008734	2D14		jmpr	cc_eq,0x875E
ok	P:008736	0845		add	r4,#0x5
taken	P:008738	3D15		jmpr	cc_ne,0x8764
		{			
never	456		case 1:		
never	457		x = x+1;		
never	P:00873A	0881	add	r8,#0x1	; x,#1
never	459		x = x*2;		
never	P:00873C	5C18	shl	r8,#0x1	; x,#1

Shadow Memory

Shadow memory can be mapped for the external bus and for the XBUS. Emulation of extra XRAM areas is possible. An 1 MByte shadow memory on

the bondout busses shows memory states on external busses, **XRAM** and **IRAM**.

- 1 MByte Shadow memory

Execution Breakpoints

The emulator supports execution breakpoints on the ROM and external area. All breakpoints are 'break-before-make' breakpoints. Emulation is stopped before execution.

- Unlimited number of software breakpoints
- Support for Onchip hardware breakpoints

HLL Debugging

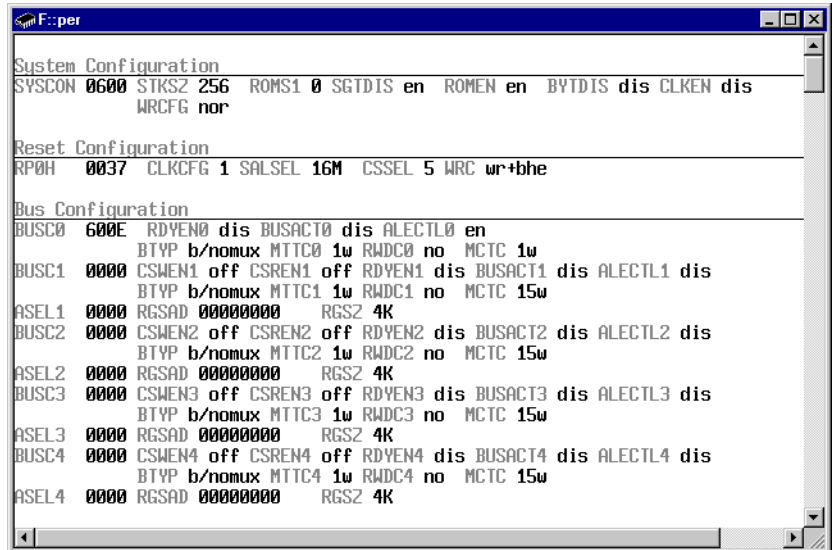
addr/line	code	label	mnemonic	comment
		int anzahl;		
141		anzahl = 0;		
P:000410	E00F	sieve:	mov r15,#0x0	
143		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;		
P:000412	E00C		mov r12,#0x0	
P:000414	E112		movb r11,#0x1	
P:000416	F0DC		mov r13,r12 ; r13,i	
P:000418	08C1		add r12,#0x1 ; i,#1	
P:00041A	E42D18FA		movb [r13+#0xFA18],r11	
P:00041E	46FC1200		cmp r12,#0x12 ; i,#18	
P:000422	BDF8		jmprr cc_sle,0x414	
145		for (i = 0 ; i <= SIZE ; i++)		
P:000424	E00C		mov r12,#0x0 ; i,#0	
147		{		
		if (flags[i])		
P:000426	F42C18FA		movb r11,[r12+#0xFA18]; r11,[i+#flags]	

Full support in real-time for:

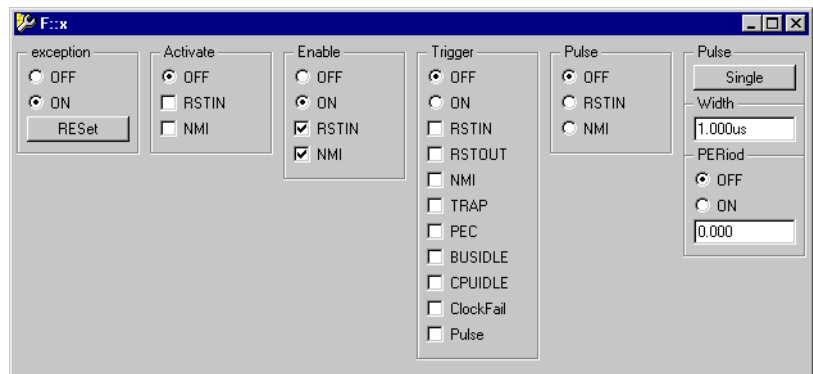
- ROM and external busses
- Break-before-line operation
- HLL single step in real-time
- Trigger and trace on local variables
- Trigger on bit variables

Voltage and Clock Monitors

- On-Line Display for SYSCON and BUSCON
- 3.3 V and 5 V Standalone operation



Exception Control



The TRACE32 exception controller allows to permanently activate an exception, to enable or disable specific exceptions, to trigger on specific exceptions or to stimulate an exception.

- Static exception setting
 - RSTIN
- Target exception control
 - RSTIN
 - NMI

- Exception trigger
 - RSTOUT
 - RSTIN
 - PWRDOWN
 - IDLE
 - TRAP
 - PEC

Port Analyzer

On the emulation base there is an extra slot for the TRACE32 Port Analyzer. The following additional signals can be traced:

- Port 0
- Port 1
- Port 2
- Port 3
- Port 4
- Port 6
- Port 7
- Port 8
- Port 9
- READY

On-Circuit Emulation

- Support for Clip-Over adapters

Emulation Modules

Modules Overview

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PowerView IDE

TRACE32-PowerView supports most compilers, realtime operation systems and debuggers.

New integrations are mostly done on customers request. If your compiler or RTOS is not supported now, please ask us !

Compiler Support

CPU	Language	Compier	Compan y	Option
C166	C	XC16X/ ST10	Cosmic Software	ELF/DWARF
C166	C	GNU- GCC166	HighTec EDV- Systeme GmbH	DBX
C166	C	C166	ARM Germany GmbH	EOMF-166
C166	C	C166	TASKIN G	IEEE
C166	C++	GNU- CPP166	HighTec EDV- Systeme GmbH	DBX
C166	C++	CP166	TASKIN G	IEEE

RTOS Support

Company	Product	Comment
ARM Germany GmbH	ARTX-166	
CMX Systems Inc.	CMX-RTX	
Elektrobit Automotive GmbH	Elektrobit tresos	via ORTI
Evidence	Erika	via ORTI
Mentor Graphics Corporation	Nucleus PLUS	
Vector	osCAN	via ORTI
Enea OSE Systems	OSE Basic	(OS166)
Enea OSE Systems	OSE Epsilon	(OS166), 3.x
-	OSEK	via ORTI
Elektrobit Automotive GmbH	ProOSEK	via ORTI
HighTec EDV- Systeme GmbH	PXROS	
ARM Germany GmbH	RTX166/-tiny	
Quadros Systems Inc.	RTXC 3.2	
Quadros Systems Inc.	RTXC Quadros	
Articus Systems AB	Rubus OS	
IBM Corp.	SDT-Cmicro	
Micrium Inc.	uC/OS-II	2.0 to 2.92

Debugger Support

CPU	Debugger	Company
	WINDOWS CE PLATF. BUILDER	-
	CODE::BLOC KS	-
	C++TEST	-
	ADENEO	-
	X-TOOLS / X32	blue river software GmbH
	CODEWRIGH T	Borland Software Corporation
	CODE CONFIDENC E TOOLS	Code Confidence Ltd
	CODE CONFIDENC E TOOLS	Code Confidence Ltd
	EASYCODE	EASYCODE GmbH
	ECLIPSE	Eclipse Foundation, Inc
	CHRONVIEW	Inchron GmbH
	LDRA TOOL SUITE	LDRA Technology, Inc.
	UML DEBUGGER	LieberLieber Software GmbH
	SIMULINK	The MathWorks Inc.
	ATTOL TOOLS	MicroMax Inc.
	VISUAL BASIC INTERFACE	Microsoft Corporation
	LABVIEW	NATIONAL INSTRUMENT S Corporation
	RAPITIME	Rapita Systems Ltd.
	RHAPSODY IN MICROC	IBM Corp.

CPU	Debugger	Company
	RHAPSODY IN C++	IBM Corp.
	DA-C	RistanCASE
	TRACEANALY ZER	Symtavigation GmbH
	TA INSPECTOR	Timing Architects GmbH
	UNDODB	Undo Software
	VECTORCAS T UNIT TESTING	Vector Software
	VECTORCAS T CODE COVERAGE	Vector Software
C166	SDT CMICRO	IBM Corp.

Operation Voltage and Frequency

The maximum operation frequency of TRACE32-FIRE depends on:

- The max. frequency of the CPU
- The access time of the overlay memory (10ns)
- The mapper mode (**Slow** or **Fast**)
- The number of waitstates
(W0 = 0 waitstates
W1 = 1 waitstate)
- The dual-port access mode
- If no emulation memory is used, the frequency limit depends on the trace speed (TRACE)
- Some probes use extra high-speed memory on the emulation adapter (HEAD RAM)

Max. Frequency with ROM and ARAM Dualport Access

Operation Voltage

This list contains information on probes available for other voltage ranges.

Probes not noted here supply an operation voltage range from 4.5V to 5.5V.

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Dimensions

Modules

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Connectors

On each emulation module there are half-size connectors to:

- Connect the emulation module directly to the target by providing the corresponding connectors also on the target hardware

- Connect a standard adapter from Emulation Technology, YAMAICHI, AMP, TOKYO ELETECH etc.

The following table lists the physical dimensions of these connectors.

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Adapter

The adapters connect in different ways

- With Clip-Over Adapters the CPU can stay on the target board.
- With Solder-ON adapters the CPU must be removed

- YAMAICHI and AMP adapters fit to the CPU socket

The following table lists the physical dimensions of these adapters.

Not necessary.

Available Tool Chain

TRACE32 provides a complete set of development tools for this family. This includes:

- The In-Circuit Emulator TRACE32-ICE
- The high speed RISC Emulator TRACE32-FIRE
- The BDM/JTAG/ONCE etc. based In-Circuit Debugger TRACE32-ICD
- The ROM Monitor based In-Circuit Debugger TRACE32-ICD
- The ICD Trace, a trace extension to the BDM/JTAG debuggers or ROM monitors
- Evaluation boards, which can be used until the target hardware is available.
- The Instruction Set Simulator (SIM), a software tool for code test without any hardware

The following list give an overview which development tools are available for the specific derivatives of this family.

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Order Information

Module Description

Detailed Order Information

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