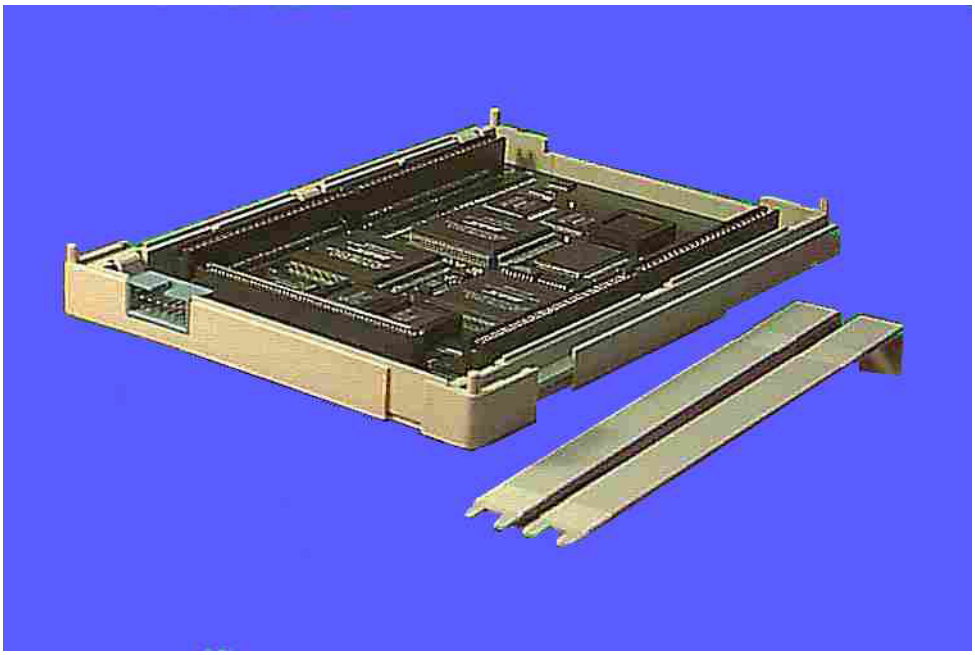
TRACE32®
Technical Information

FIRE-EMUCON



FIRE Emulation Controller

- Universal Emulation Controller
- 16 .. 64 Bit Support
- 160 Channel Trace Analyzer
- 64/512K Trace Depth
- Time-Stamp 10ns
- Statistic Analyzer
- Performance Analyzer
- Trigger System
- VCO 1..150 MHz

The FIRE-EMUCON is the universal emulation system for all FIRE emulation probes.

The system includes the general emulator functions like trigger system and runtime control system.

The trigger system enables complex trigger functions on address breakpoints, on events and external signals. An trigger output for external DSOs or logic analyzers is available.

An analyzer system with 160 trace channels, time stamp and performance analyzer capability is included in this module.

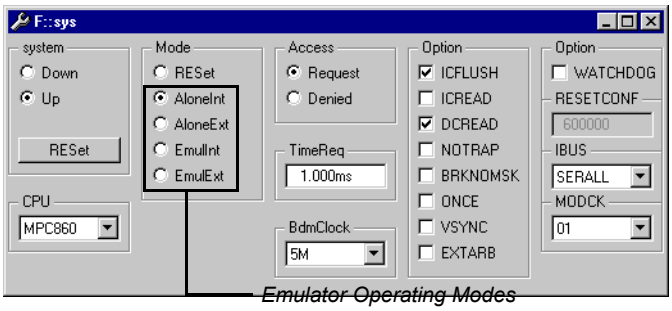
21.02.17

LAUTERBACH
DEVELOPMENT TOOLS

In-Circuit Emulator

Most Emulation Functions can be used while the target CPU is running ('on the fly' operation)

Two Emulator Operating Modes



Emulator Operating Modes

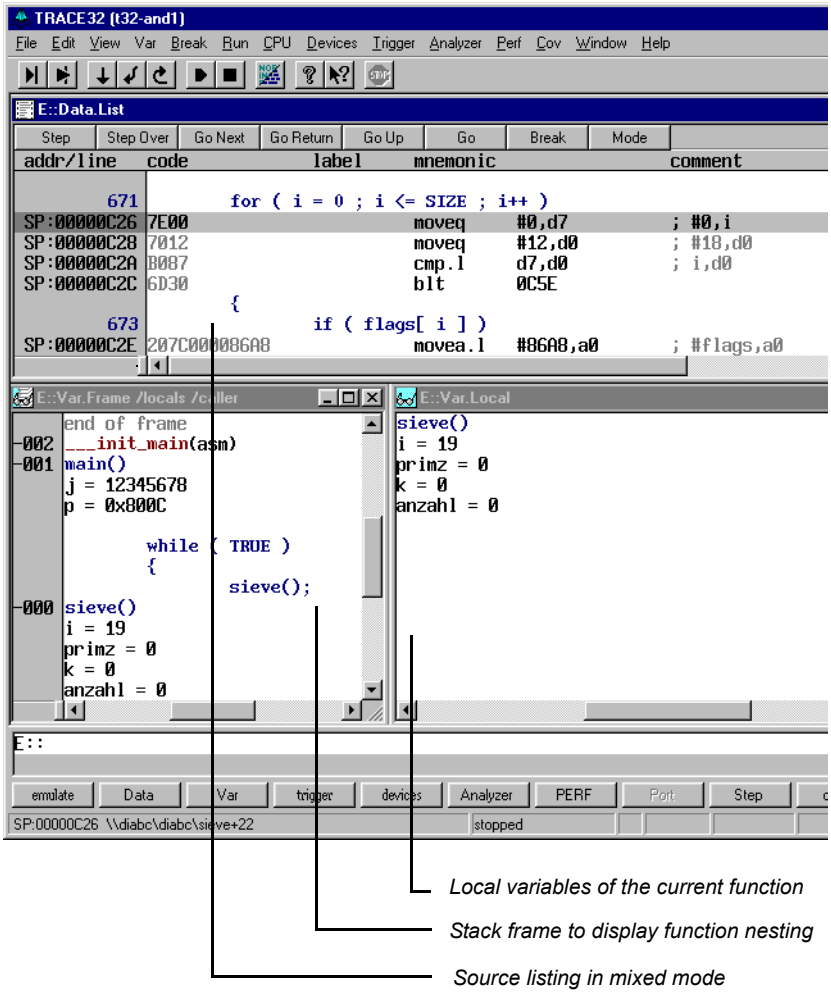
Stand Alone Mode

The emulator operates without being connected to the target system. In this mode all emulator capabilities can be used for software debugging.

Active Mode

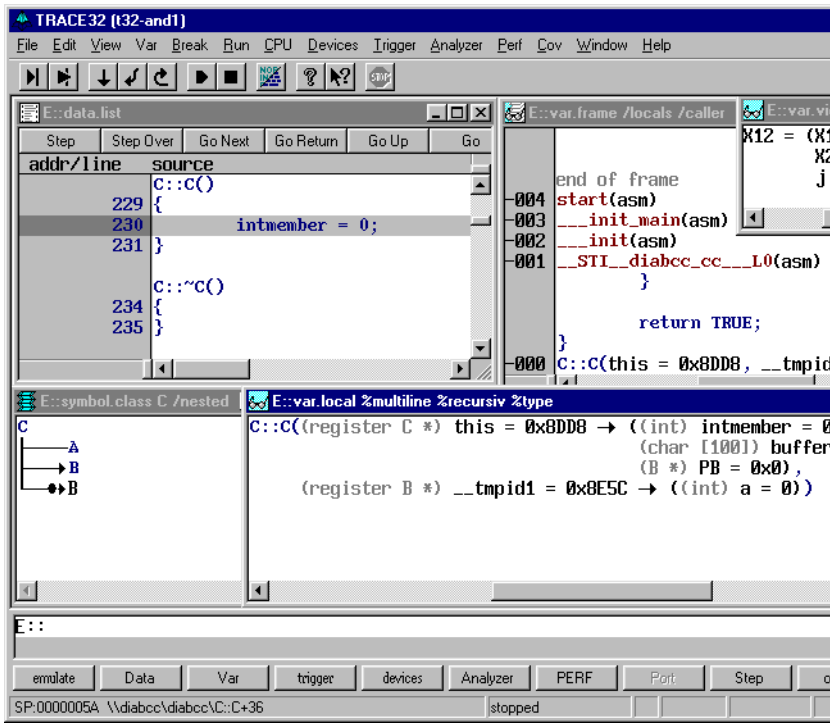
The emulator operates with the target system (with internal or external clock). This mode provides the ability to test software and hardware using all the functions of TRACE32.

Symbolic Debugging



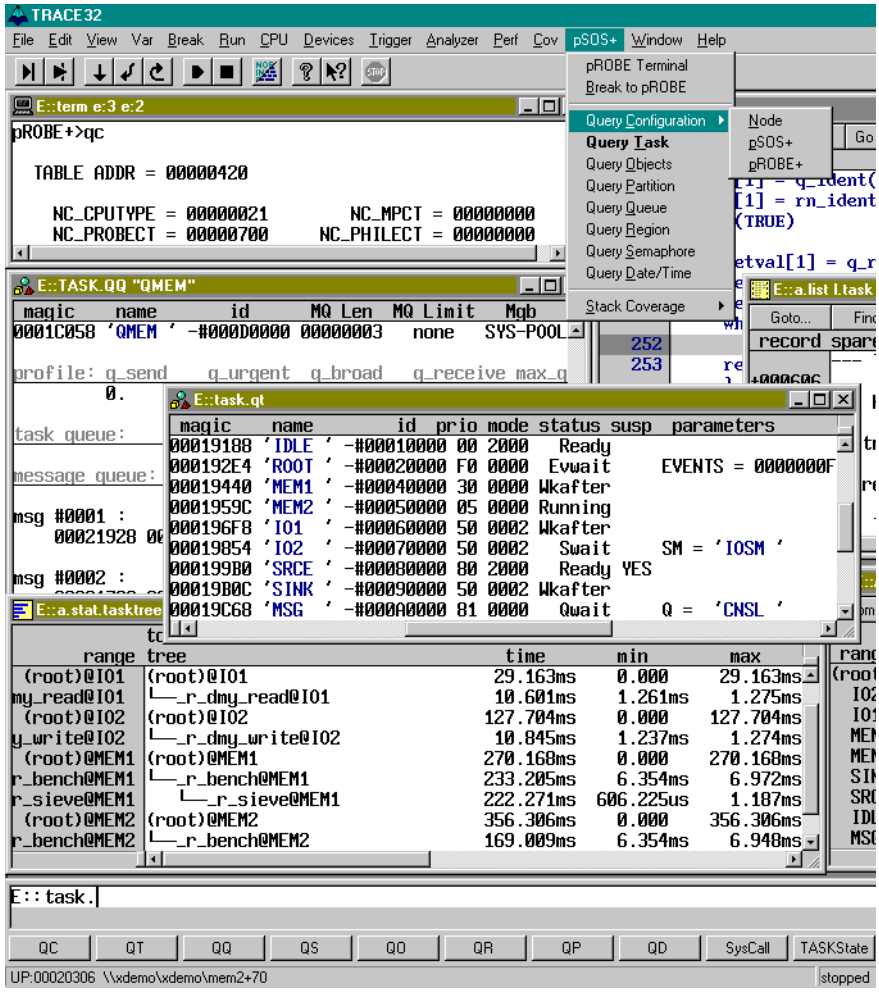
A hierarchical symbol database enables structured symbolic debugging. Symbol names can be up to 255 significant characters long and can be used to show single program addresses, module names and memory classes. The disassembler can use the symbols for labels and/or operands. Demangling for C++ signatures is supported.

High-Level Language Debugging



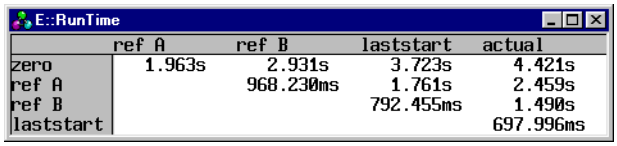
TRACE32 can directly load the output of all standard compilers for C, C++, Pascal, Modula2, PEARL and ADA from most compiler vendors. Program display and debugging can be done in assembler, high-level or in a mixture of both. It is possible to construct both assembler and high-level windows on the screen simultaneously. All variable types specific to the high-level language can be displayed and modified. Addresses can be absolute, relative or line number based.

Multitask Debugging



The TRACE32 multitask debugger supports all common RTOS. The multitask debugger supports symbolic debugging of complex multi-task applications and the detailed analysis of the real time behaviour of the system.

Runtime Analyzer

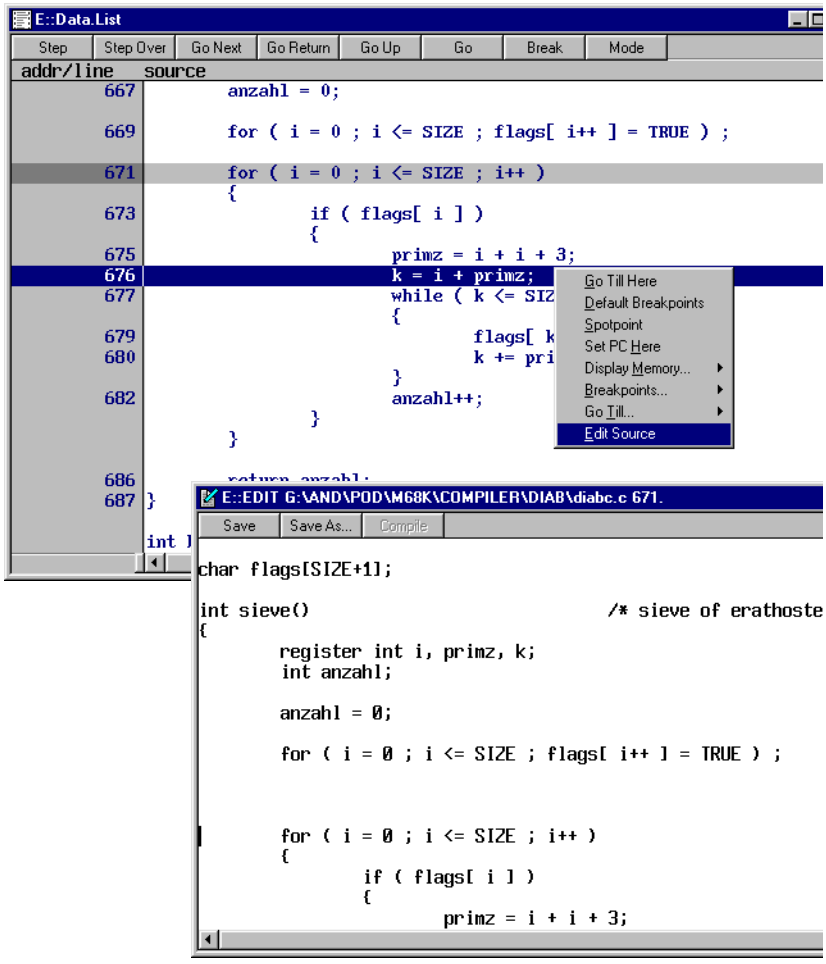


Program runtime is recorded automatically.

- Time from initial start - 300ns to 300 days

- ❑ Time from the last program stop - 100ns to 300 days
- ❑ Time difference between 3 reference points - 300ns to 300 days
- ❑ Timers can be checked at any time

Edit/Debug Link



The editor window can be synchronised to the debugging window so that when an error is found, the source text can immediately be shown and if required, edited.

On-Screen Assembler

The on-screen assembler is provided in addition to the more common inline assembler found on other systems. With the on-screen

assembler, short programs can be written quickly and reliably. It is not a full assembler whose output code is linkable to the main program in the usual way .

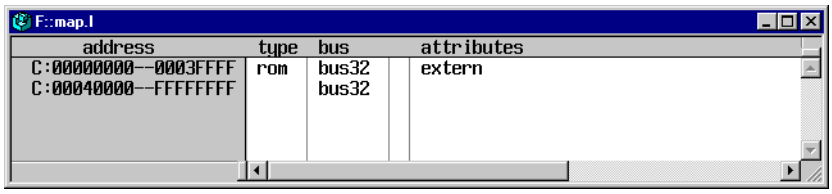
Up to 16 MByte Emulation RAM

To store programs in the emulator during the development phase, the emulator provides up to 16 Mbyte overlay memory . This memory can be static SRAMs with an access time of down 3 ns. (typ 10 ns).

Dual-Ported Access to all Emulation Memory

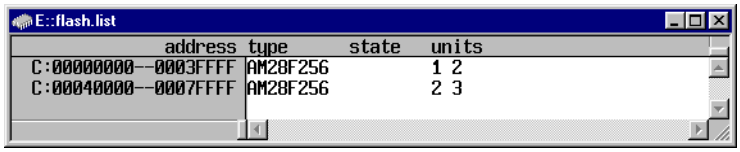
The whole emulation memory system is dual-ported. This allows the emulator to read or write memory while the target system is running in real-time e.g. to show variables, port contents etc. For low to medium CPU clock frequencies there is no decrease in performance of the target system due to the operation of the dual-port access mechanism. At higher CPU clock frequencies, the performance may be slightly reduced in accordance with the number of accesses made by the control system. The dual-port access mechanism can be switched off, but if this is done, then memory access by the emulator can only take place when the target program is stopped.

Selective Mapping of Memory Classes



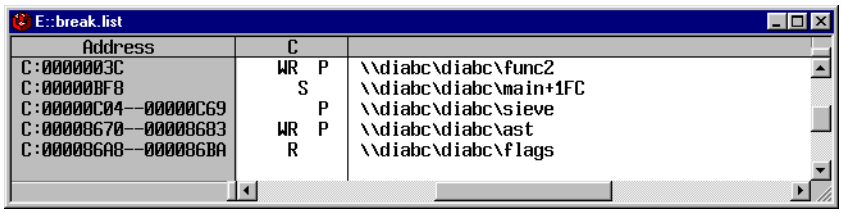
The address mapper can segment the memory into 4 segments. By using this segmentation, it is possible for example to split the memory so that a PROGRAM area can be mapped to the emulator RAM while the DATA area remains mapped as target memory. It is also possible to have totally separate physical memory areas displayed simultaneously.

Flash Programming



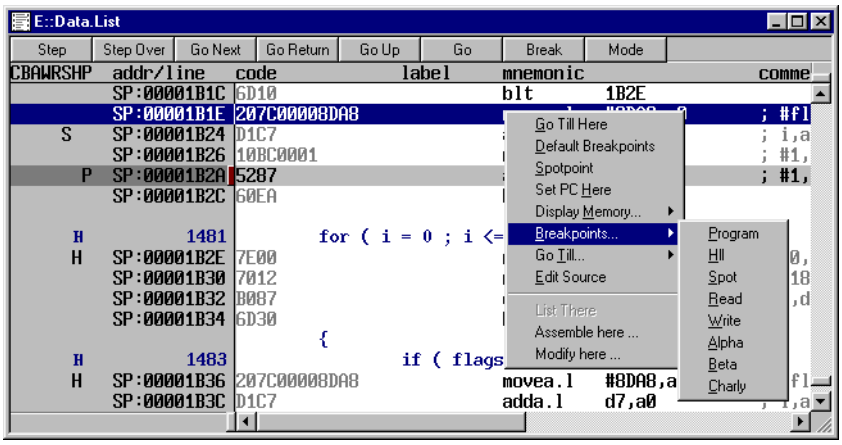
TRACE32 supports the programming of external flash memory as well as the programming of internal flash memory of microcontrollers. The programming can be controlled by the emulator or by a routine in the target system.

Memory Oriented Breakpoint System with up to 16 MByte Breakpoint Memory



Most currently available emulators use multiple address and data comparators to form the breakpoint system. This technique not only restricts the number of breakpoints available it also means that systems using bank selection are difficult to support. The breakpoint memory on the TRACE32 is basically a bytewide memory structure that can be mapped in a similar way like the overlay memory. When any memory location is accessed, the corresponding breakpoint byte is also accessed so that there are effectively 8 kinds of breakpoints for each addressable location.
The break memory is dual-ported, so that breakpoints can be set and displayed while the system is running.

9 Breakpoint Types



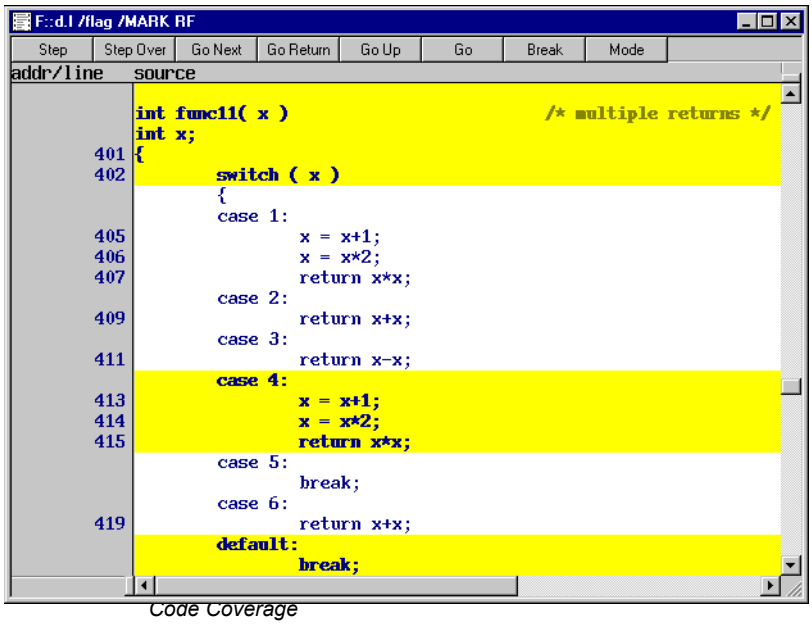
- ❏ Program Breakpoint
- ❏ Spot Breakpoint
- ❏ Data Read Breakpoint
- ❏ Data Write Breakpoint
- ❏ General Purpose Point A..E

In each group there are up to 16 million breakpoints available depending upon the amount of breakpoint ram in the emulator. Breakpoints can be specified as a single address or an address range.

Support for On-Chip Breakpoints

On-Chip breakpoint system are used to generate hardware break-points.

Flag System

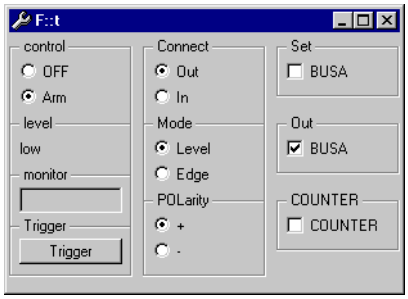


Code Coverage

In a special memory, all addresses which are read or written are marked with read or write flags. This memory can therefore supply a lot of important information:

- ❏ Systematic program test due to the fact that each executed module will be marked in the flag ram.
- ❏ Detection of unused or unexecuted code.
- ❏ Systematic system test through visible code coverage analysis.
- ❏ Detecting accesses to unused or illegal address locations.

Bus Trigger System



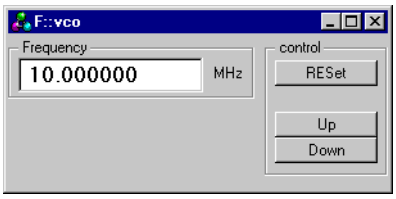
- ❏ Trigger interactions with other TRACE32 systems
- ❏ Change trigger polarity

Strobe Monitor for Target System

If the strobe period becomes >>10µs the system will alert the user. If programmed to do so, the emulator can go into a standby mode if this occurs .

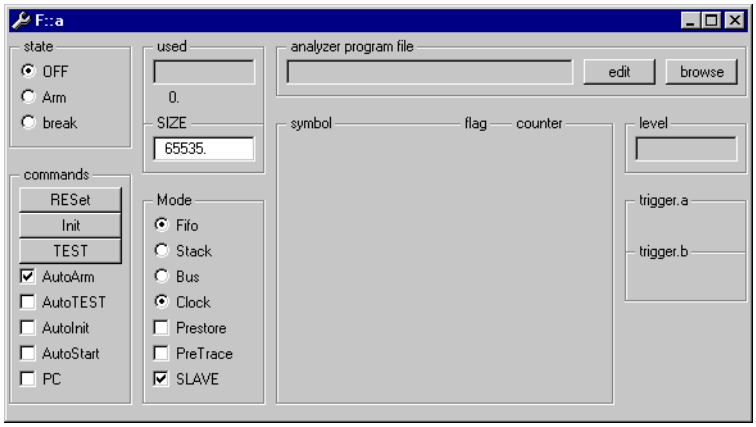
Internal Frequency Generator

- ❏ Variable VCO with frequency range from 1 to 150 MHz.
- ❏ Emulation CPU clock frequency programming is done via the emulation control unit.



State Analyzer

Operation Modes



- ❏ 160 Trace Channels
- ❏ Up to 320 Extra Trace Channals on Emulator Module
- ❏ High-Speed 10ns Cycle Time
- ❏ Clock and Bus Trace
- ❏ Large Trace Depth (64K/ 512KFrames)
- ❏ Trace Memory Depth programmable from 0.1 K to 512 K
- ❏ Two Operating Modes - FIFO and STACK
- ❏ Freely defined Markers can also be recorded to highlight specific Routines
- ❏ Time Correlation available with Logic Analyzer and ICD Trace or other Emulators

Internal Expansion Capability

External Trigger Inputs

- ❏ 2 external inputs

Free Format Definition of Data Events

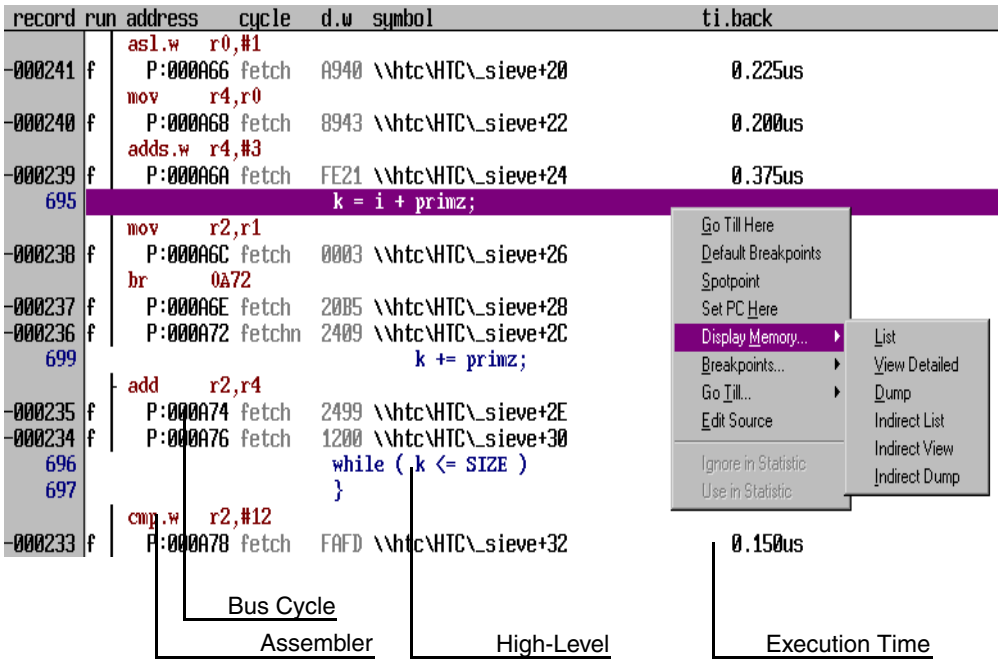
Data events can be specified with constants, masks, or

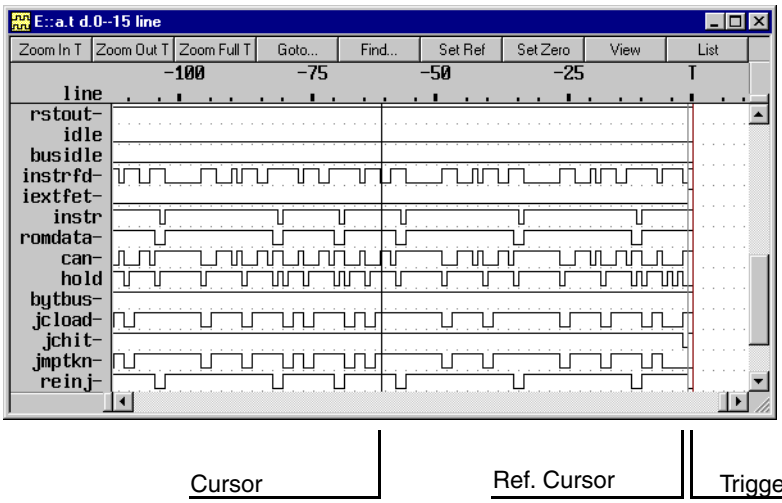
boolean formulae.

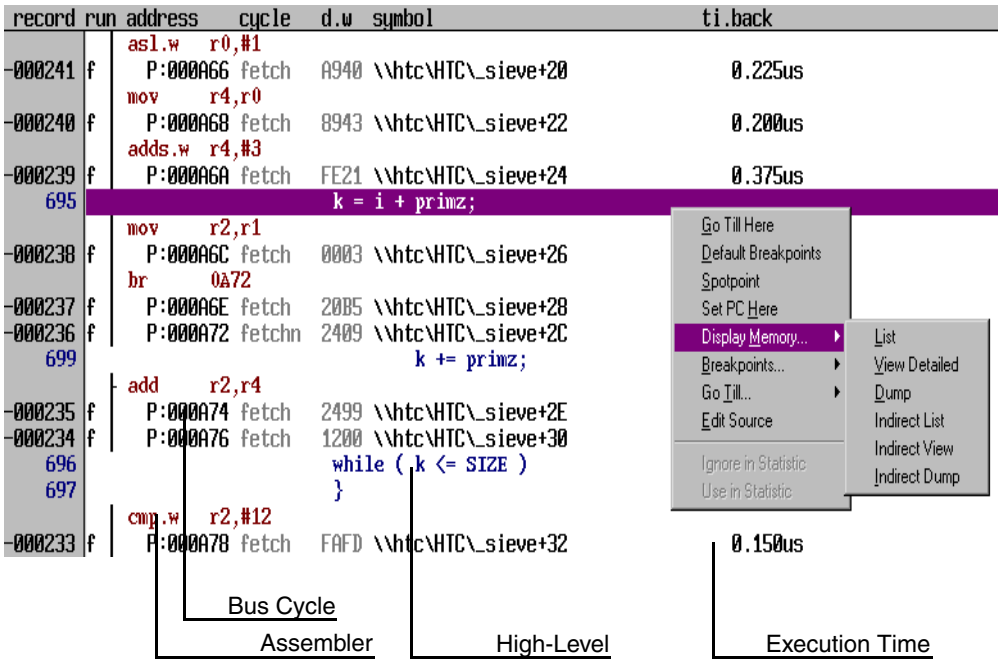
Hex and Mnemonic Display of Trace Data

Configurable Display

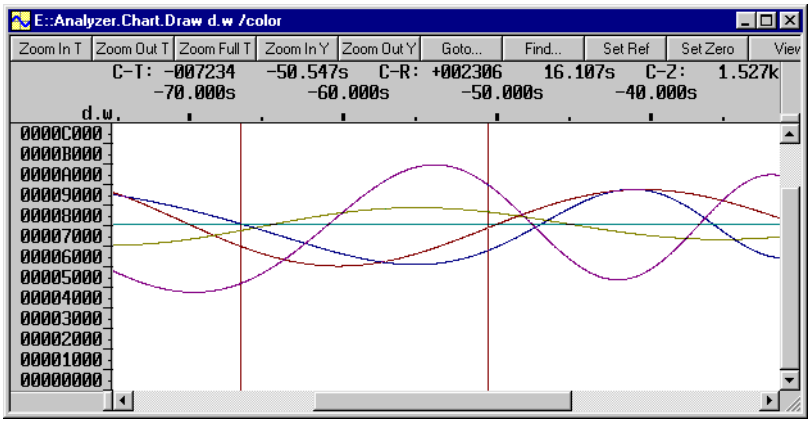
- ❏ Dissassembly or HII
- ❏ Special Channels
- ❏ Ascii/Hex/Decimal/Bin
- ❏ Suppress Prefetching
- ❏ Dequeued Disassembly




E::a.t d.0--15 line
Zoom In T
Zoom Out T
Zoom Full T
Goto...
Find...
Set Ref
Set Zero
View
List
-100
-75
-50
-25
T
line
rstout-
idle
busidle
instrfd-
iextfet-
instr
romdata-
can-
hold
bytbus-
jcload-
jchit-
jmptkn-
reinj-
Cursor
Ref. Cursor
Trigger

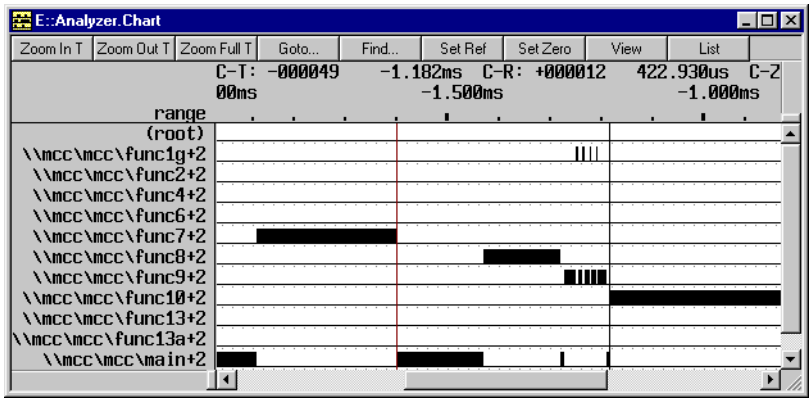

record run address cycle d.w symbol ti.back
asl.w r0,#1
-000241 f P:000A66 fetch A940 \\htc\HTC_sieve+20 0.225us
mov r4,r0
-000240 f P:000A68 fetch 8943 \\htc\HTC_sieve+22 0.200us
adds.w r4,#3
-000239 f P:000A6A fetch FE21 \\htc\HTC_sieve+24 0.375us
695 k = i + primz;
mov r2,r1
-000238 f P:000A6C fetch 0003 \\htc\HTC_sieve+26
br 0A72
-000237 f P:000A6E fetch 20B5 \\htc\HTC_sieve+28
-000236 f P:000A72 fetchn 2409 \\htc\HTC_sieve+2C
699 k += primz;
add r2,r4
-000235 f P:000A74 fetch 2499 \\htc\HTC_sieve+2E
-000234 f P:000A76 fetch 1200 \\htc\HTC_sieve+30
696 while (k <= SIZE)
697 }
cmp.w r2,#12
-000233 f P:000A78 fetch FAFD \\htc\HTC_sieve+32 0.150us
Go Till Here
Default Breakpoints
Spotpoint
Set PC Here
Display Memory...
Breakpoints...
Go Till...
Edit Source
Ignore in Statistic
Use in Statistic
List
View Detailed
Dump
Indirect List
Indirect View
Indirect Dump
Bus Cycle
Assembler
High-Level
Execution Time

Graphic Display



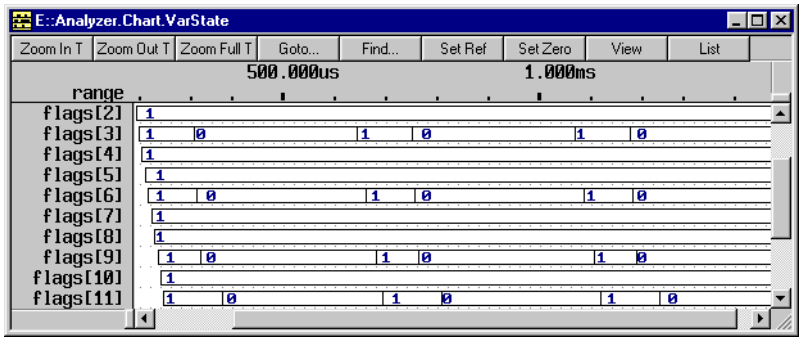
Graphical Display

❑



Execution Time Chart

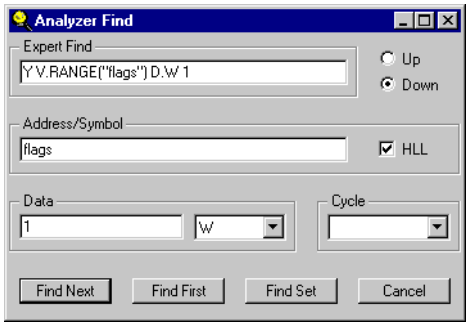
❑



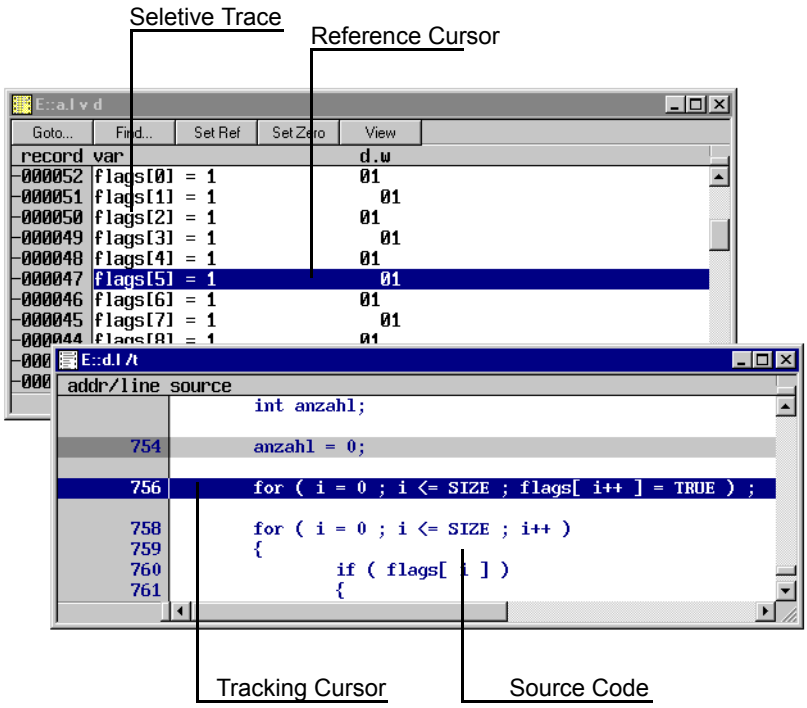
Variable Time Chart

Powerful Trace Memory Manager

- ❏ Save memory
- ❏ Load memory
- ❏ Print memory
- ❏ Compare memory
- ❏ Find specific entry
- ❏ Goto record
- ❏ Time and record number evaluation.
- ❏ Referenz pointer
- ❏ User defined display



Tracking to List Windows



Graphical Data Display

- ❏ Show A/D Conversion
- ❏ Visualize Program Flow

Complex Search and Compare Functions

Save and Reload of Trace Data

PC Display on Real-Time Emulation

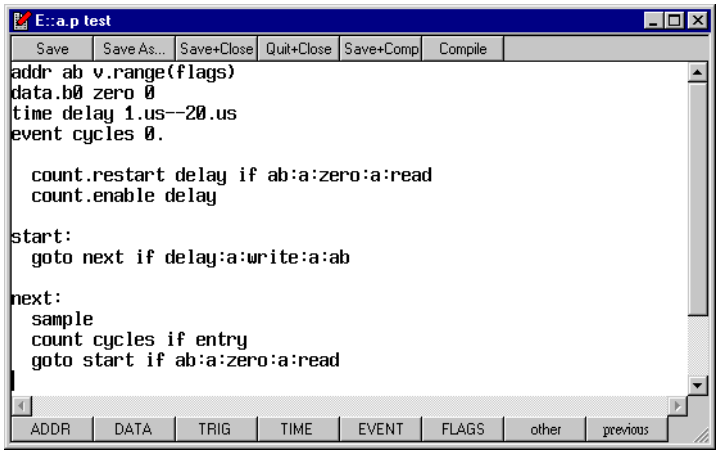
Trigger Unit

Main Trigger Unit with 4 Levels

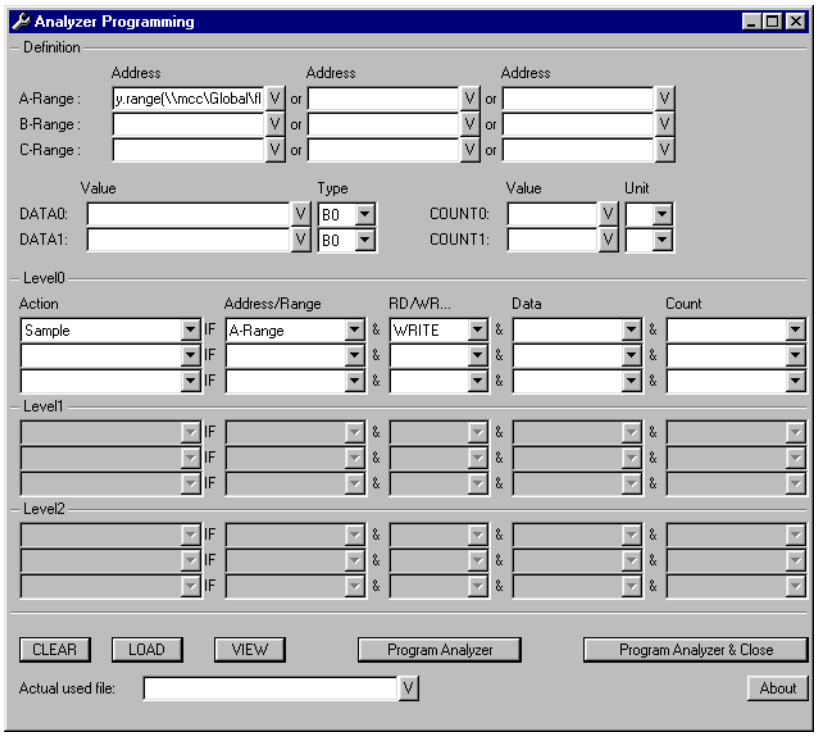
The level structure of the trigger unit allows very flexible trigger combinations and sequences in consecutive and nonconsecutive order. Each level has the same priority and the same capabilities. A trigger program defines, under which circumstances a level can be reached or left, and therefore which trigger conditions or operations are the current or the next.

Analyzer Programming via a special Window

The programming of this complex trigger unit is done in an assembler like language for maximum flexibility. Using this language, the programming of very complex trigger sequences or operations can be defined. For simple demands, a pull down menu improves the programming for beginners.



Fast Programming by Menu



Symbolic Operations for Analyzer Programming

All output operators and input variables can be entered in symbolic form. The target program symbols can also be used.

Trigger Sources

- ❏ 4 hardware breakpoints
- ❏ 1 data events (mask, range, ASCII, hex, binary)
- ❏ 2 external trigger events
- ❏ CPU state (MEM READ, IO WRITE, INTA, ...)
- ❏ Counter outputs

External Trigger Inputs

- ❏ 2 inputs lines
- ❏ 2 trigger qualifiers for each trigger level
- ❏ Static levels of the trigger inputs can be read at any time
- ❏ Free format definition of external trigger events

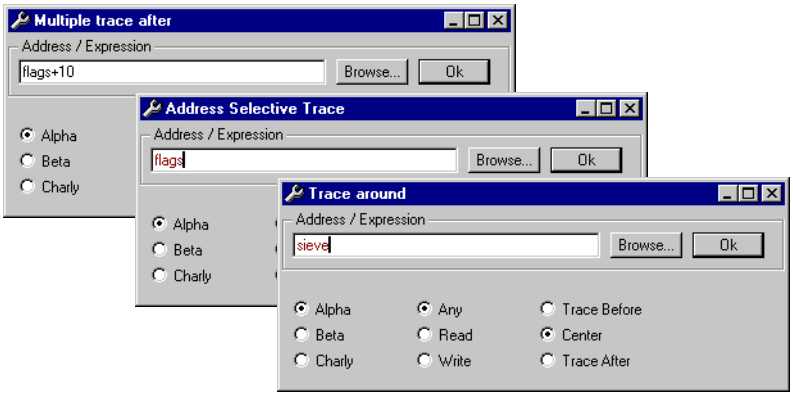
Trigger Output Operations

- Count.Restart
- Count.Enable
- Sample.Enable
- Break Program
- Trigger.Exception
- Out (Target Stimulation)
- Break Analyzer
- Bus.Trigger
- Spot
- GOTO level
- Mark record

Free Format Definition of Data, Address and Trigger Events

- Hex and hex masks
- Binary and binary masks
- ASCII character and string

Wizzards for Standard Trigger Problems



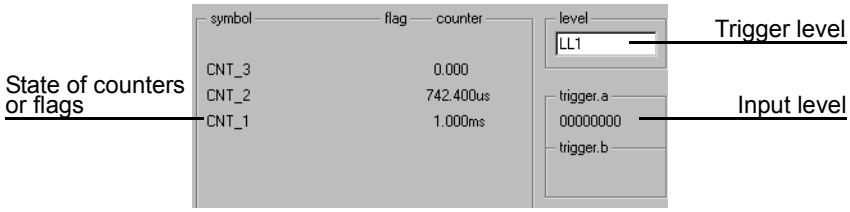
Time and Event Measurements with up to 3 Counters

There are 2 28-bit counters and 2 28-bit Timers available for event measurement or event triggering. All counters are re-triggerable and can be evaluated as a part of an expression in the trigger sequences. Each counter can be programmed as a timer for timing measurements or an event counter.

- Retriggerable
- Selective release
- Trigger event when counter is zero
- Definition of time and event windows
- All Counters can be read 'on the fly'

Trigger Monitor

A display of the counter values, the trigger values, the trigger levels and the trigger flags is available in the trigger monitor window.



Statistic Analyzer

❑ Time Stamp

The Time Stamp Unit tags each trace record with a time value. These values are absolute and synchronized with all the other time values within the TRACE32 system.

❑ Recording depth max. 64/512K

❑ 48 time stamp recording channels

❑ Resolution 20ns

❑ Maximum measuring time 1.3 days

Function Analysis

❑ Min. and max. time

❑ Passes

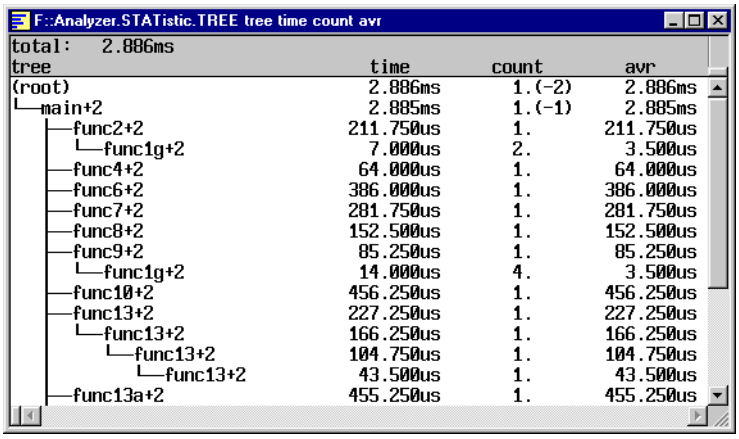
❑ Include and exclude time

Link Analysis

❑ Callers

❑ Min. and max. times

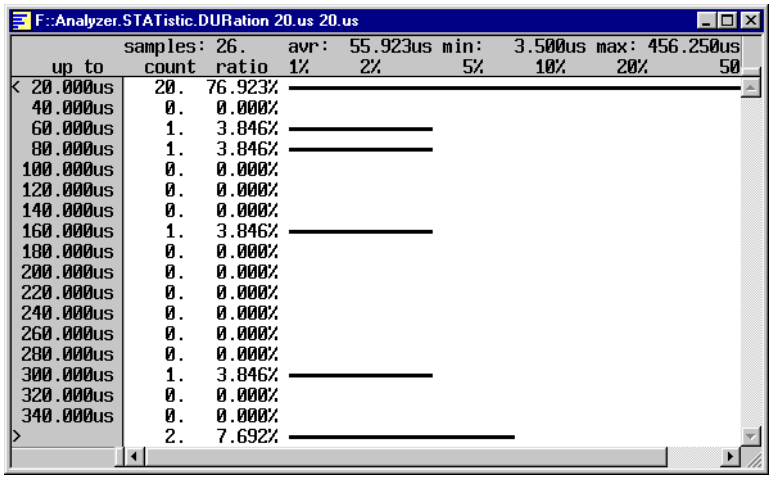
❑ Calls



Duration

❑ Execution time

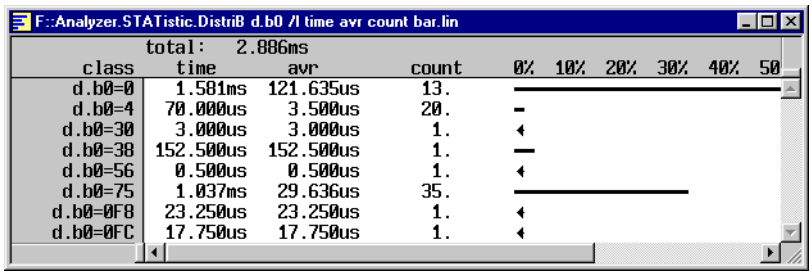
❑ Response time



Distance

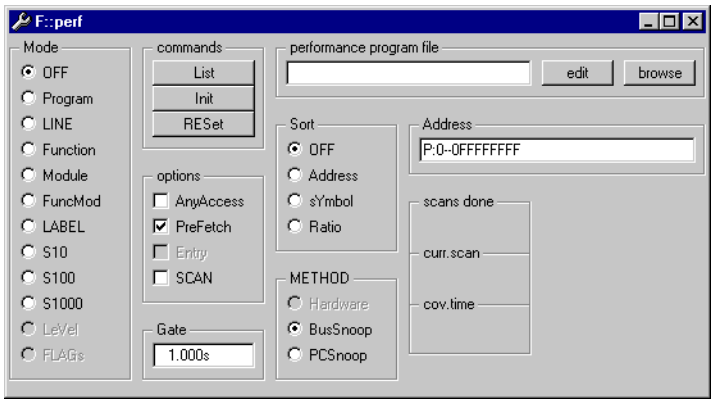
❑ Time between samples

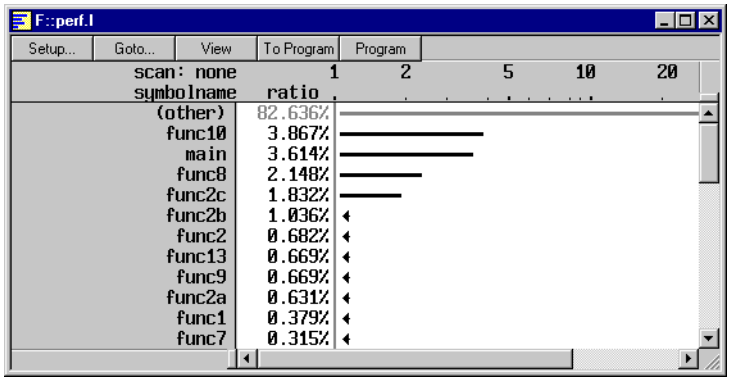
Distribution



Performance Analyzer

- Resolution
  - 100 us
  - Statistic Reatime Messurement
- Performance Address Ranges
  - Modules
  - Functions
  - Address ranges





Order Information

Module Description

Detailed Order Information

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