*Timing Analyzer (optional)**ICE-Base**High Speed State Analyzer***Emulation Controller Unit***System Controller Unit*

## Emulation Controller Unit for 8 ... 32-Bit

- Universal for all 8- to 32-bit CPUs
- Mapper with 1 Byte Resolution
- Trigger System
- Frequency Generator
- Universal Counter
- Pulse Generator
- Code Coverage
- Slot for static emulation memory card with up to 2MByte overlay and 2MByte break memory
- Slot for Shadow RAM
- Upgrade with SRAM up to 16 MByte emulation memory
- 4 probe connectors on the front side for external banking, trigger and runtime control signals
- 3 BNC connectors on the back side

## In-Circuit Emulator

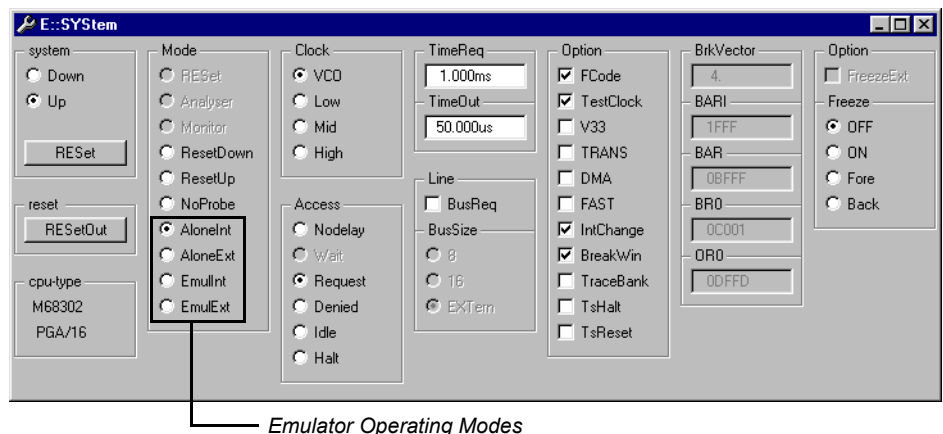
### Separate Emulation Control Processor

The emulator is controlled by a separate processor. Functions such as task changing or memory refresh

are done independently of the main system controller or the emulation CPU.

### Most Emulation Functions can be used while the target CPU is running ('on the fly' operation)

### Two Emulator Operating Modes



Emulator Operating Modes

### Stand Alone Mode

The emulator operates without being connected to the target system. In this mode all emulator capabilities can be used for software debugging.

### Active Mode

The emulator operates with the target system (with internal or external clock). This mode provides the ability to test software and hardware using all the functions of TRACE32.

## Symbolic Debugging

The screenshot shows the TRACE32 debugger interface with three main windows:

- Top Window (E::Data.List):** Displays assembly code in mixed mode. The code includes a loop: `for ( i = 0 ; i <= SIZE ; i++ )`. The assembly instructions shown are: `moveq #0,d7 ; #0,i`, `moveq #12,d0 ; #18,d0`, `cmp.l d7,d0 ; i,d0`, `blt 0C5E`, and `movea.l #86A8,a0 ; #flags,a0`.
- Middle Window (E::Var.Frame /locals /caller):** Shows a stack frame for the `sieve()` function. It lists local variables: `i = 19`, `prinzh = 0`, `k = 0`, and `anzahl = 0`. The stack frame also shows the function's call site within a `while ( TRUE )` loop.
- Bottom Window (E::):** Shows the source code listing for the `sieve()` function, which matches the assembly code above: `sieve()`, `i = 19`, `prinzh = 0`, `k = 0`, `anzahl = 0`, `while ( TRUE )`, `{`, `sieve();`, `}`.

Local variables of the current function

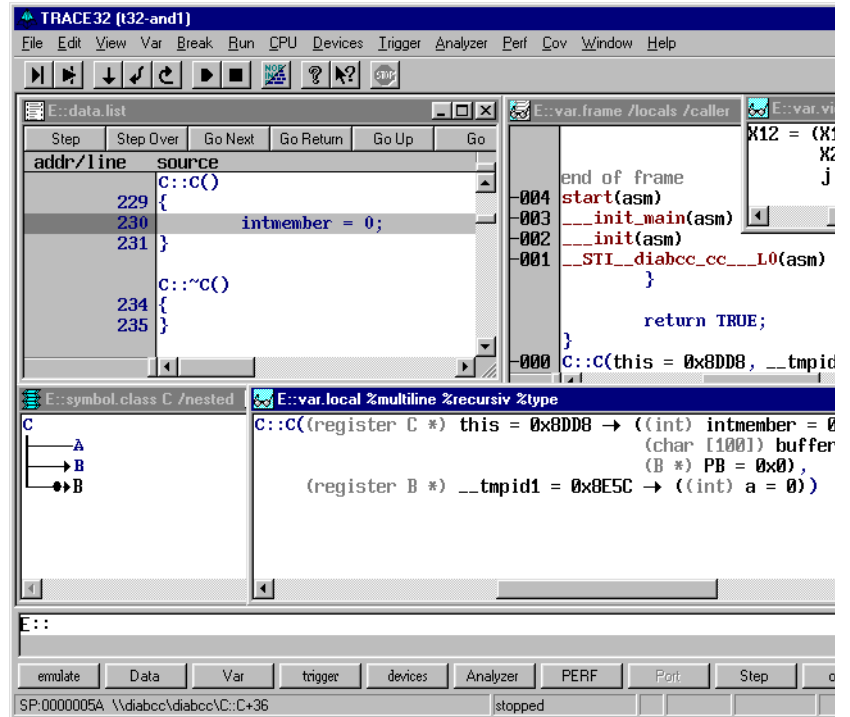
Stack frame to display function nesting

Source listing in mixed mode

A hierarchical symbol database enables structured symbolic debugging. Symbol names can be up to 255 significant characters long and can be used to show single program addresses, module names

and memory classes. The disassembler can use the symbols for labels and/or operands. Demangling for C++ signatures is supported.

## High-Level Language Debugging



TRACE32 can directly load the output of all standard compilers for C, C++, Pascal, Modula2, PEARL and ADA from most compiler vendors. Program display and debugging can be done in assembler, high-level or in a mixture of both. It is

possible to construct both assembler and high-level windows on the screen simultaneously. All variable types specific to the high-level language can be displayed and modified. Addresses can be absolute, relative or line number based.

## Multitask Debugging

The screenshot displays the TRACE32 multitask debugger interface. The main window shows the command prompt with the command 'pROBE+>qc' and the output of the 'qc' command, which lists system parameters such as ADDR, NC\_CPUYPE, NC\_MPCT, NC\_PROBECT, and NC\_PHILECT. Below this, the 'E::TASK.QQ "QMEM"' window shows a table of memory queues with columns for magic, name, id, MQ Len, MQ Limit, and Mqb. The 'E::task.qt' window displays a task queue table with columns for magic, name, id, prio, mode, status, susp, and parameters. The 'E::a.stat.tasktree' window shows a task tree with columns for range, tree, time, min, and max. The bottom of the interface includes a toolbar with buttons for QC, QT, QQ, QS, QO, QR, QP, QD, SysCall, and TASKState, and a status bar showing the current session path and state.

The TRACE32 multitask debugger supports all common RTOS. The multitask debugger supports symbolic debugging of complex multi-

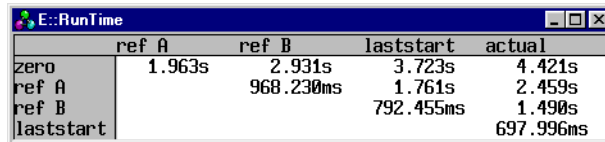
task applications and the detailed analysis of the real time behaviour of the system.

## Background Task

For systems that require certain aspects of their operation to be maintained at all times (e.g. interrupts, timer operations etc.), a background program can be executed so that these real-time dependencies can be serviced. The

application (foreground task) is then debugged in the normal manner. When the foreground task is stopped, the background program still performs all necessary services in real time.

## Runtime Analyzer



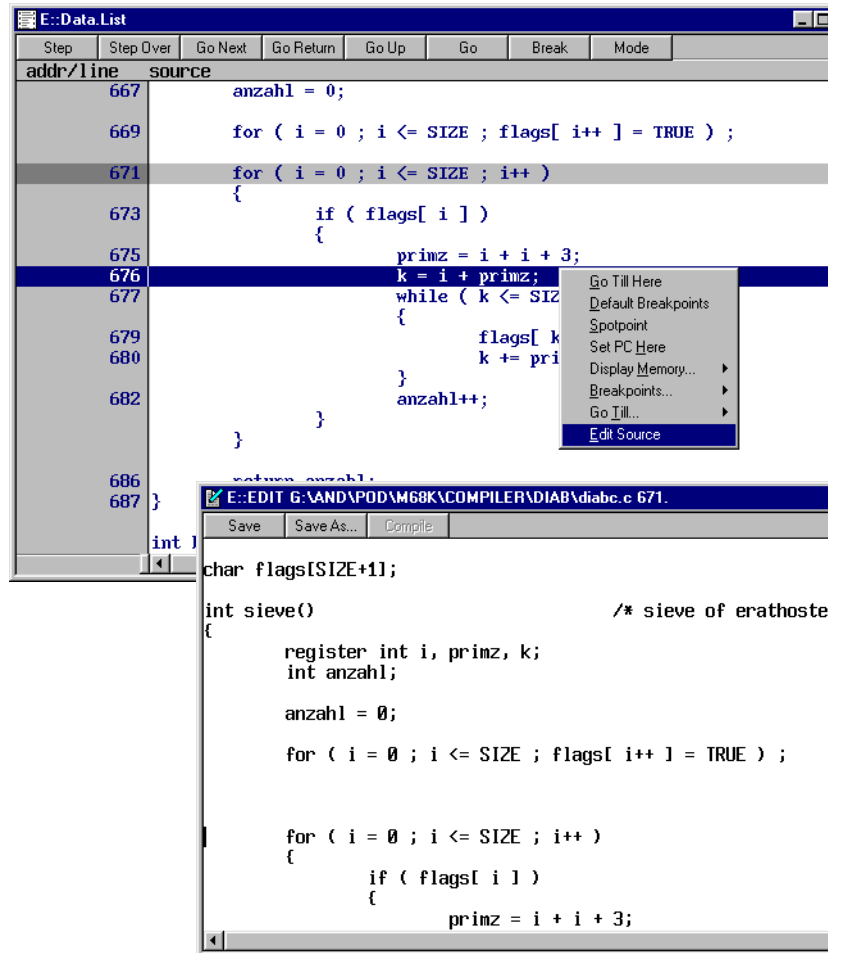
	ref A	ref B	laststart	actual
zero	1.963s	2.931s	3.723s	4.421s
ref A		968.230ms	1.761s	2.459s
ref B			792.455ms	1.490s
laststart				697.996ms

Program runtime is recorded automatically.

- Time from initial start - 300ns to 300 days
- Time from the last program stop - 100ns to 300 days

- Time difference between 3 reference points - 300ns to 300 days
- Timers can be checked at any time

## Edit/Debug Link



The editor window can be synchronised to the debugging window so that when an error is found, the source text can immediately be shown and if required, edited.

## On-Screen Assembler

The on-screen assembler is provided in addition to the more common inline assembler found on other systems. With the on-screen assembler, short programs can be

written quickly and reliably. It is not a full assembler whose output code is linkable to the main program in the usual way .

---

## 16 MByte Emulation RAM

To store programs in the emulator during the development phase, the emulator provides up to 16 Mbyte

overlay memory. This memory can be static RAMs with an access time of 35ns or 15ns or dynamic RAMs.

---

## Dual-Ported Access to all Emulation Memory

The whole emulation memory system is dual-ported. This allows the emulator to read or write memory while the target system is running in real-time e.g. to show variables, port contents etc. For low to medium CPU clock frequencies (e.g. 20 MHz at 68302) there is no decrease in performance of the target system due to the operation of the dual-port access mechanism.

At higher CPU clock frequencies, the performance may be slightly reduced in accordance with the number of accesses made by the control system. The dual-port access mechanism can be switched off, but if this is done, then memory access by the emulator can only take place when the target program is stopped.

---

## Option 256 KByte Shadow RAM

The shadow RAM offers dual-port read access and RAM coverage test for high speed CPUs with no restrictions.

Shadow RAM can be mapped in 64K blocks.

---

## Option Dualport RAM

An dual-ported RAM for microcontroller applications is available. The memory allows dual-ported access during realtime application at high-

est speed and zero wait states with microcontrollers like C167, H8 or 80196, where no bus arbitration is available.

---

## Memory Mapping in 4K Blocks and bitwise

The main mapping of memory is done in 4K/512K blocks. However within a 32K block, mapping can

also be performed down to a single byte resolution (useful for I/O mapping).



## Selective Mapping of Memory Classes

Address	UP			UD			SP			SD		
	Attr	Ram	Wait	Attr	Ram	Wait	Attr	Ram	Wait	Attr	Ram	Wait
00000000--00007FFF	I		Fds			Fds	I		Fds			Fds
00008000--000090FF	I		Ds	I		Ds	I		Ds	I		Ds
00009100--00009FFF			Ds			Ds			Ds			Ds
0000A000--0000A002				I		Ds				I		Ds
0000A003--0000AFFF						Ds						Ds

The address mapper can segment the memory into 4 segments. By using this segmentation, it is possible for example to split the memory so that a PROGRAM area can be mapped to the emulator RAM while

the DATA area remains mapped as target memory. It is also possible to have totally separate physical memory areas displayed simultaneously.

## Wait States and Write Protection

0 to 250 wait cycles can be specified within any particular address range.

Data access in specific address areas can be prevented. Using this feature for example, it is possible to

prevent an I/O access occurring at a specific address (if bitwise mapping is operative).

Address	UP			UD			SP			Attr
	Attr	Ram	Wait	Attr	Ram	Wait	Attr	Ram	Wait	
00000000--0000FFFF	IP		Fds	IP		Fds	IP		Fds	IP
00001000--00007FFF										
00008000--00008FFF			Fds	2		Fds	2		Fds	2
00009000--00009014			Fds			Fds			Fds	
00009015--0000A014	P		Fds	P		Fds	P		Fds	P
0000A015--0000AFFF			Fds			Fds			Fds	

## Support for External Bank Switching (up to 256 banks)

External bank switching schemes or MMUs can be supported by the memory mapper. For this there are separate probe inputs to the emula-

tor. This option is only sensible on CPUs with less than 16 Mbyte addressing range.

## Support for EPROMs with Inbuilt Paging

EPROMs of the types 27513 or 27011 are supported without external logic. The address area within

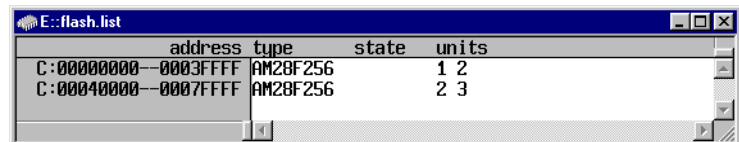
the EPROM has to be defined by the user, so that the emulator can support the device.

## Support for Dynamic Memory in the Target System

In order to refresh target dynamic RAM when the emulation is stopped, a memory refresh function

is provided. The address range and memory class over which the refresh occurs can be defined.

## Flash Programming

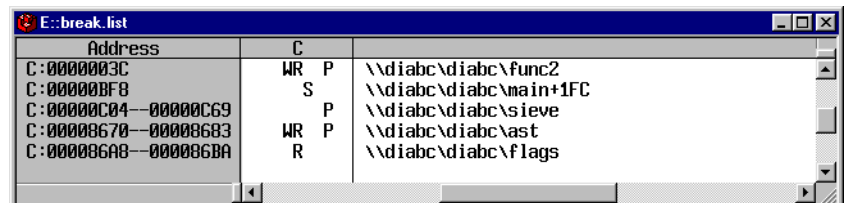


address	type	state	units
C:00000000--0003FFFF	AM28F256		1 2
C:00040000--0007FFFF	AM28F256		2 3

TRACE32 supports the programming of external flash memory as well as the programming of internal flash memory of microcontrollers.

The programming can be controlled by the emulator or by a routine in the target system.

## Memory Oriented Breakpoint System with up to 16 MByte Breakpoint Memory



Address	C	
C:0000003C	WR	P \\diabc\diabc\func2
C:00000BF8		S \\diabc\diabc\main+1FC
C:0000C04--0000C69		P \\diabc\diabc\sieve
C:0000B670--0000B6B3	WR	P \\diabc\diabc\ast
C:0000B6A8--0000B6BA		R \\diabc\diabc\flags

Most currently available emulators use multiple address and data comparators to form the breakpoint system. This technique not only restricts the number of breakpoints available it also means that systems using bank selection are difficult to support. The breakpoint memory on the TRACE32 is basically a byte-wide memory structure that can be mapped in a similar way

like the overlay memory. When any memory location is accessed, the corresponding breakpoint byte is also accessed so that there are effectively 8 kinds of breakpoints for each addressable location.

The break memory is dual-ported, so that breakpoints can be set and displayed while the system is running.



## Flag System

The screenshot shows a window titled 'E::Flag.ListFunc'. It contains two main sections:

symbol name	read	write	read only	write only	read
abc\diabc\func8					100 %
abc\diabc\func9					100 %
bc\diabc\func10					100 %
bc\diabc\func11					37 %
bc\diabc\func13					100 %
bc\diabc\func14					100 %
bc\diabc\func15					100 %

addr./line	code	label	mnemonic	
SP:00000840	4EB900001984		jsr	1984
SP:00000846	6008		bra	850
		case 5:	break;	
		case 6:	return x+x;	
457				
SP:00000848	2007		move.l	d7,d0
SP:0000084A	0000		add.l	d0,d0
SP:0000084C	6002		bra	850
		default:	break;	
		}		
461		return x;		
SP:0000084E	2007		move.l	d7,d0
462		}		

Code Coverage

In a special memory, all addresses which are read or written are marked with read or write flags. This memory can therefore supply a lot of important information:

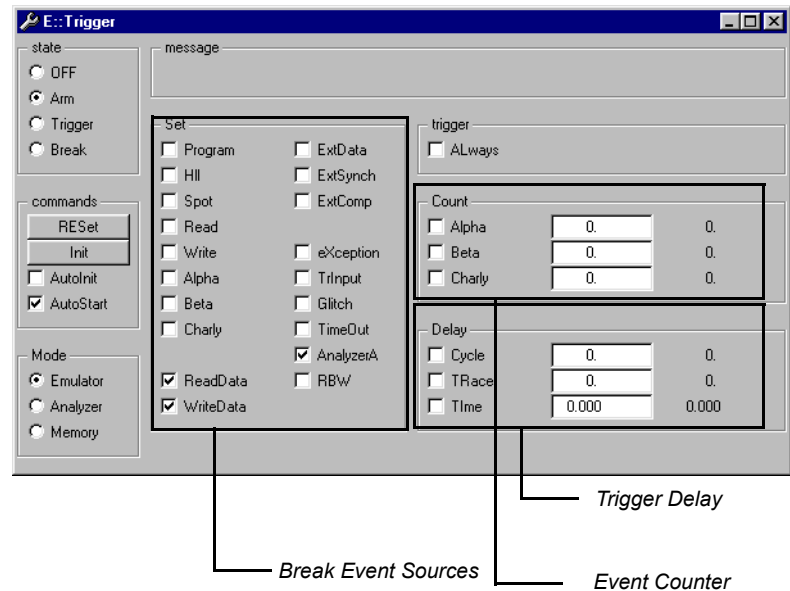
- Detection of uninitialised memory.
- Reading of uninitialised memory can be forced to generate an automatic break or to trigger the trace analyzer.
- Systematic program test due to the fact that each executed module will be marked in the flag ram.
- Detection of unused or unexecuted code.
- Systematic system test through visible code coverage analysis.
- Detecting accesses to unused or illegal address locations.

## Trigger Outputs

8 trigger/status outputs are provided. These outputs are mainly intended for triggering or controlling certain functions within the target system. External analyzers can be triggered using the Trace Analyzer outputs.

- Emulator trigger output
- Emulator RUN and cycle signal
- Address signal from the breakpoint memory
- Pulse generator output
- Universal counter output

## Break Event Sources



- |   |   |
|---|---|
| <input type="checkbox"/> Normal breakpoint            | <input type="checkbox"/> Exception break (e.g. RESET, NMI etc.) |
| <input type="checkbox"/> High-level breakpoint        | <input type="checkbox"/> Analyzer break A                       |
| <input type="checkbox"/> Data read breakpoint         | <input type="checkbox"/> Bus timeout (TimeOut)                  |
| <input type="checkbox"/> Data write breakpoint        | <input type="checkbox"/> Glitch Detector                        |
| <input type="checkbox"/> General purpose breakpoint A | <input type="checkbox"/> Synchronous external trigger event     |
| <input type="checkbox"/> General purpose breakpoint B | <input type="checkbox"/> Asynchronous trigger event             |
| <input type="checkbox"/> General purpose breakpoint C | <input type="checkbox"/> ReadBeforeWrite                        |

## Delayed Trigger

A trigger delay between the trigger event and the emulation break can be specified in terms of time, a cycle count or trace cycle count.

- Time delay 100ns to 300 days
- Cycles 0 to 2.8 E+14
- Trace cycles 0 to 2.8 E+14  
The triggering can either stop the target CPU or only the recording in the trace buffer.

## Event Counter

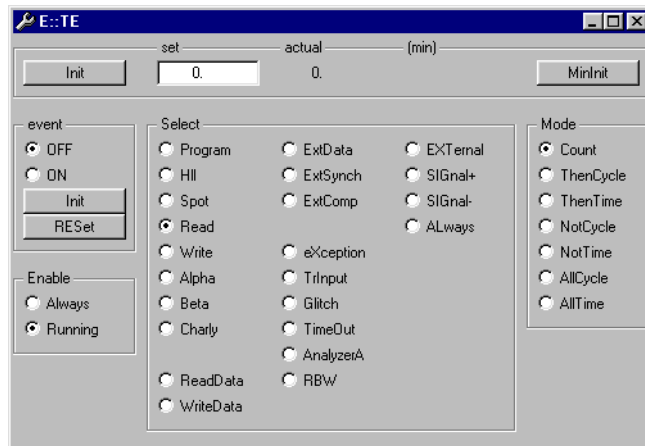
Each of the general purpose breakpoints A, B & C has an associated 48 bit counter. Using these counters it is possible to break not at the first, but at the nth trigger event.

## Bus Timeout

A timeout for bus cycles to the target system can be defined. The cycle time can be within a range of

10 $\mu$ s to 10s. Expiry of the timeout period can be used to generate an emulator break.

## Event Trigger



All trigger sources can also be selected as the source for the event trigger unit. The following trigger modes are possible:

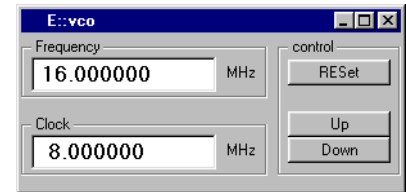
- Direct Trigger
- Trigger after N (1 .. 2.8E+14) cycles delay
- Trigger after T (100ns .. 300days) time delay
- Trigger after N events
- Delay trigger event fo N cycles
- Delay trigger event for T time
- Trigger if the specified trigger event does not happened within M (1 .. 65535) cycles
- Trigger if the specified trigger event does not happened within T time

## Strobe Monitor for Target System

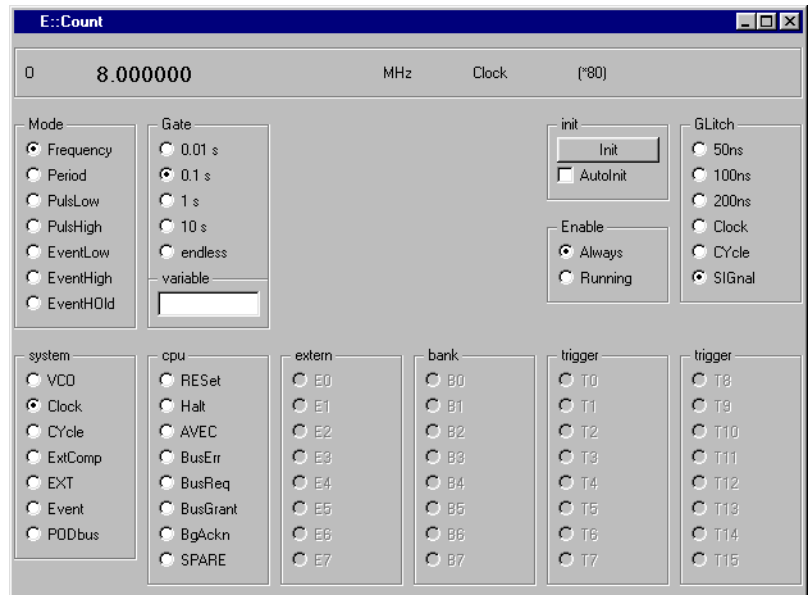
If the strobe period becomes  $\gg 10\mu$ s the system will alert the user. If programmed to do so, the emulator can go into a standby mode if this occurs .

## Internal Frequency Generator

- Variable VCO with frequency range from 1 to 70 MHz.
- No phase change when frequency changed - this can be used to test the limiting frequencies of the target system. Output available for direct connection to the target system (BNC).
- Emulation CPU clock frequency programming is done via the emulation control unit.



## Integrated Universal Counter



- Frequency 0 to 20MHz
- System clock 0 to 80MHz
- Pulse width 100ns to 300 days
- Positive or negative edge count
- 0 to 2.8E + 14
- Use for measuring of internal and external signals like cycle frequency, CPU clock frequency, interrupt frequency etc.

## Inbuilt GLITCH-Detector for all important CPU signals

- Detection of glitches down to 5ns wide within a CPU cycle
- Break at glitch detection

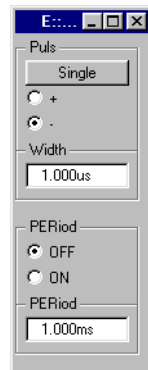
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## Profiler

- Data transfer rates
- Interrupt rates
- System performance

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## Built-in Pulse Generator



- Pulse width 100ns to 6.5ms
- Single shot mode via keypress  
Break Monitor





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## Order Information

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### Module Description

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### Detailed Order Information

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