TRACE32®

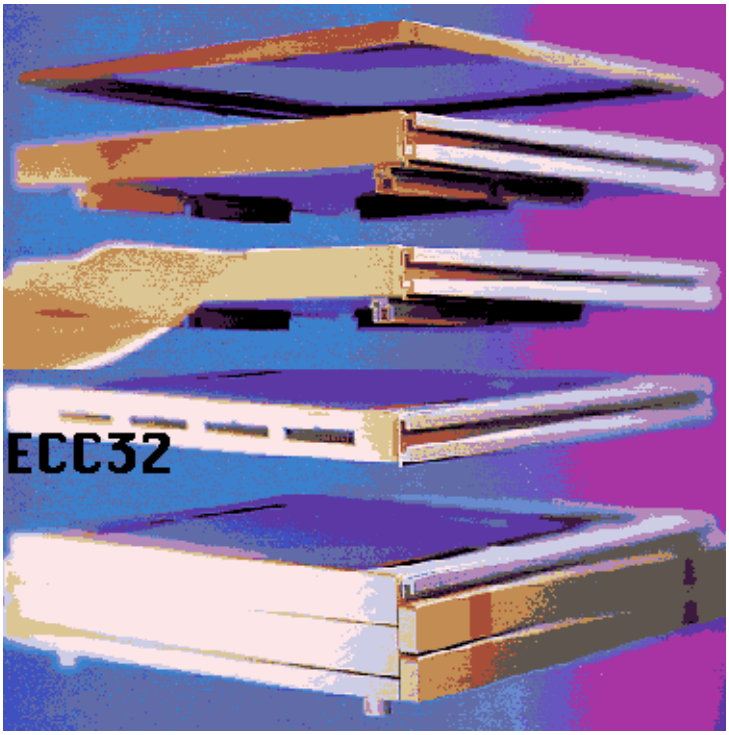
Technical Information

Emulation Memory (optional)

ICE-Base

Emulation Controller Unit

System Controller Unit



32 Bit Emulation Compact Controller

- Universal Emulation Controller
- 8 .. 32 Bit Support
- Mapper
- Trigger System
- Banking Support
- Code Coverage
- Universal Counter
- Pulse Generator
- VCO
- Trace Analyzer
- Performance Analyer

The ECC32 is the universal emulation system for all ICE emulation probes.

The system includes the general emulator functions like mapper, trigger system and runtime control system. The banking system supports emulation up to 16 MByte with 256 bank. The universal mapper can support mirroring and splitting for every 4K area. 4 different memory classes with each 16 MByte are supplied by the mapper.

ECC32

21.02.17

The trigger system enables simple trigger functions on address breakpoints, on events and external signals. An trigger output for external DSOs or logic analyzers is available.

Additional many support systems like universal counter, VCO, pulse generator and glitch detector allow easy emulation and bug detection in complex applications.

An analyzer system with 120 trace channels, time stamp and performance analyzer capability is included in this module.

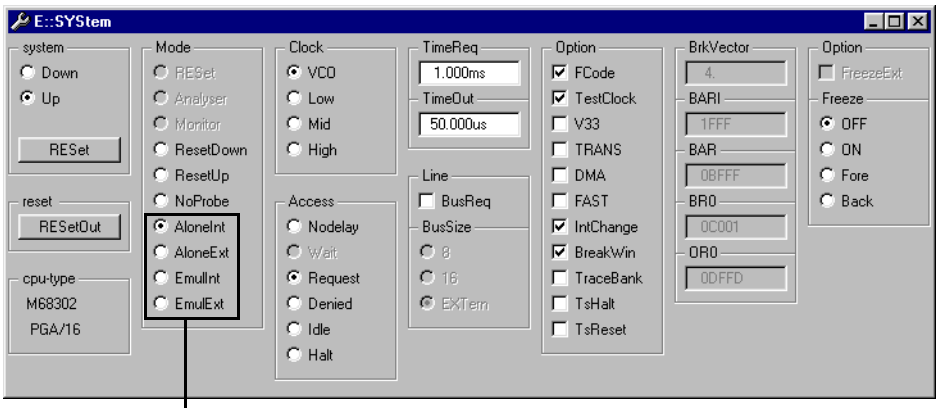
In-Circuit Emulator

Separate Emulation Control Processor

The emulator is controlled by a separate processor. Functions such as task changing or memory refresh are done independently of the main system controller or the emulation CPU.

Most Emulation Functions can be used while the target CPU is running ('on the fly' operation)

Two Emulator Operating Modes



Emulator Operating Modes

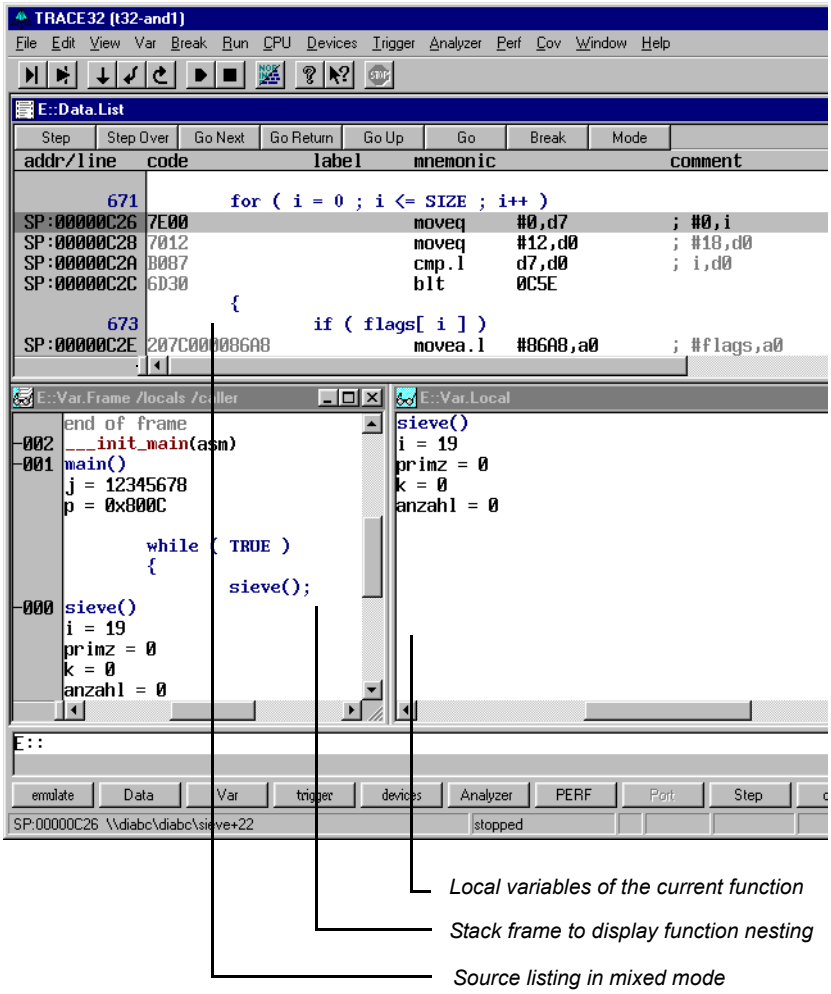
Stand Alone Mode

The emulator operates without being connected to the target system. In this mode all emulator capabilities can be used for software debugging.

Active Mode

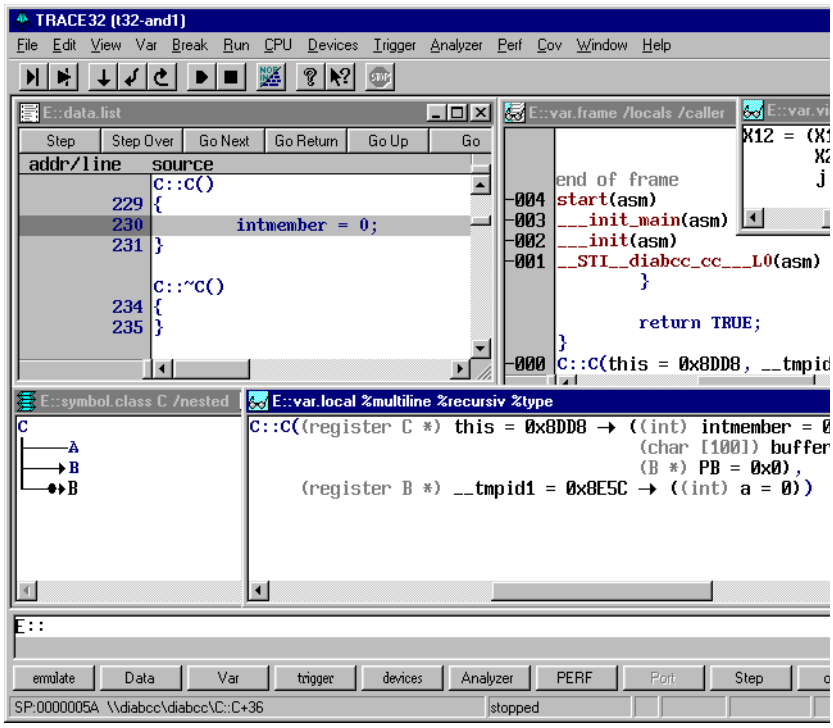
The emulator operates with the target system (with internal or external clock). This mode provides the ability to test software and hardware using all the functions of TRACE32.

Symbolic Debugging



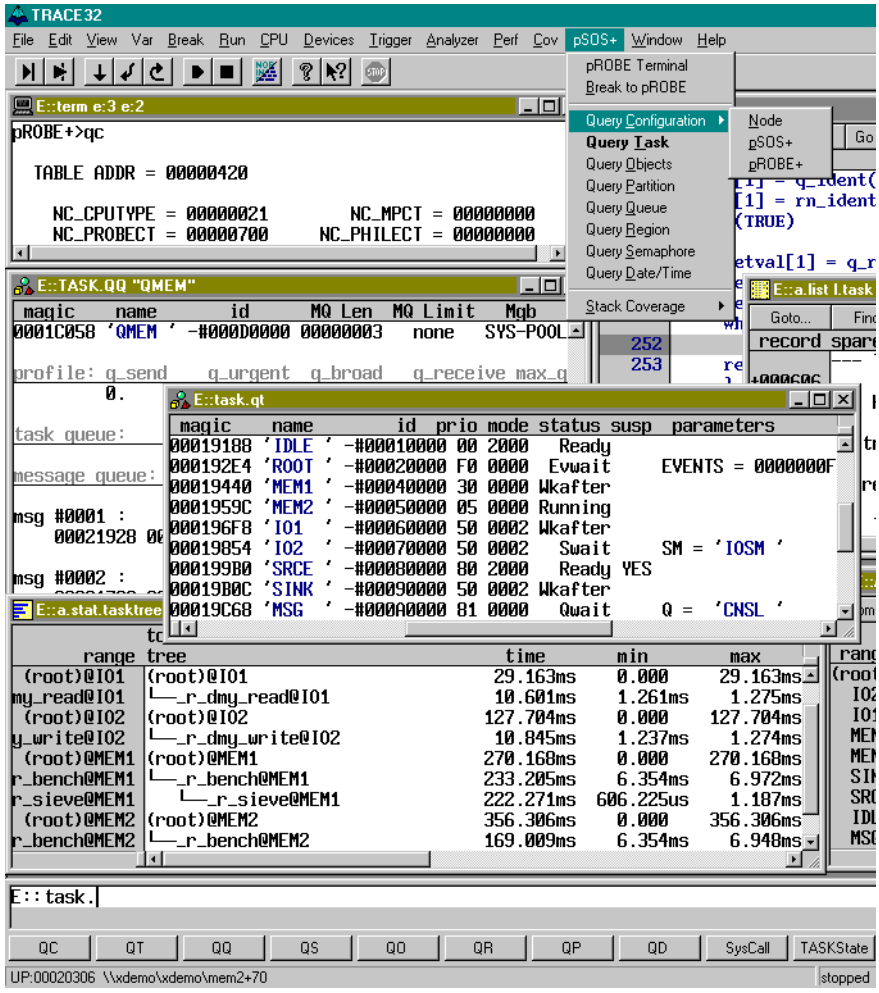
A hierarchical symbol database enables structured symbolic debugging. Symbol names can be up to 255 significant characters long and can be used to show single program addresses, module names and memory classes. The disassembler can use the symbols for labels and/or operands. Demangling for C++ signatures is supported.

High-Level Language Debugging



TRACE32 can directly load the output of all standard compilers for C, C++, Pascal, Modula2, PEARL and ADA from most compiler vendors. Program display and debugging can be done in assembler, high-level or in a mixture of both. It is possible to construct both assembler and high-level windows on the screen simultaneously. All variable types specific to the high-level language can be displayed and modified. Addresses can be absolute, relative or line number based.

Multitask Debugging

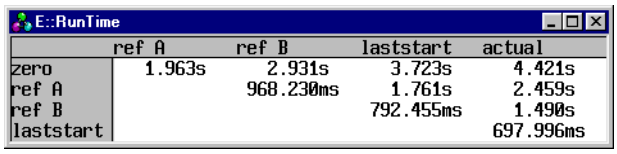


The TRACE32 multitask debugger supports all common RTOS. The multitask debugger supports symbolic debugging of complex multi-task applications and the detailed analysis of the real time behaviour of the system.

Background Task

For systems that require certain aspects of their operation to be maintained at all times (e.g. interrupts, timer operations etc.), a background programs can be executed so that these real-time dependencies can be serviced. The application (foreground task) is then debugged in the normal manner. When the foreground task is stopped, the background program still performs all necessary services in real time.

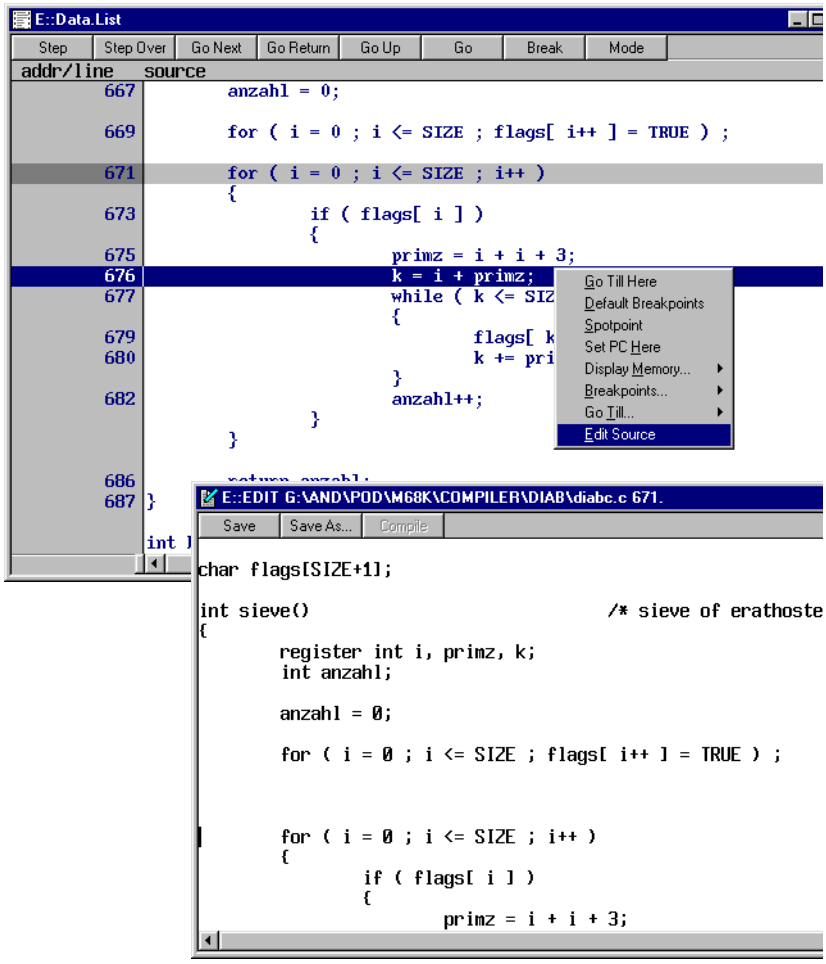
Runtime Analyzer



Program runtime is recorded automatically.

- Time from initial start - 300ns to 300 days
- Time from the last program stop - 100ns to 300 days
- Time difference between 3 reference points - 300ns to 300 days
- Timers can be checked at any time

Edit/Debug Link



The editor window can be synchronised to the debugging window so that when an error is found, the source text can immediately be shown and if required, edited.

On-Screen Assembler

The on-screen assembler is provided in addition to the more common inline assembler found on other systems. With the on-screen assembler, short programs can be written quickly and reliably. It is not a full assembler whose output code is linkable to the main program in the usual way .

16 MByte Emulation RAM

To store programs in the emulator during the development phase, the emulator provides up to 16 Mbyte overlay memory . This memory can be static RAMs with an access time of 35ns or 15ns or dynamic RAMs.

Dual-Ported Access to all Emulation Memory

The whole emulation memory system is dual-ported. This allows the emulator to read or write memory while the target system is running in real-time e.g. to show variables, port contents etc. For low to medium CPU clock frequencies (e.g. 20 MHz at 68302) there is no decrease in performance of the target system due to the operation of the dual-port access mechanism. At higher CPU clock frequencies, the performance may be slightly reduced in accordance with the number of accesses made by the control system. The dual-port access mechanism can be switched off, but if this is done, then memory access by the emulator can only take place when the target program is stopped.

Option 256 KByte Shadow RAM

The shadow RAM offers dual-port read access and RAM coverage test for high speed CPUs with no restrictions.

Shadow RAM can be mapped in 64K blocks.

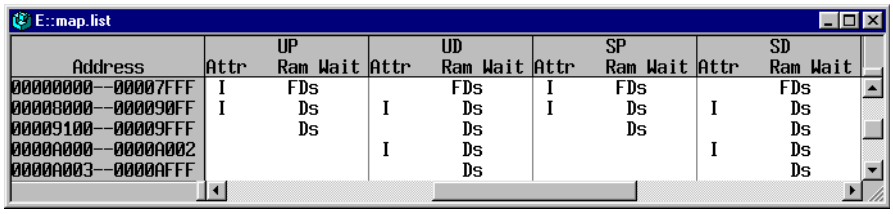
Option Dualport RAM

An dual-ported RAM for microcontroller applications is available. The memory allows dual-ported access during realtime application at highest speed and zero wait states with microcontrollers like C167, H8 or 80196, where no bus arbitration is available.

Memory Mapping in 4K Blocks and bytewise

The main mapping of memory is done in 4K/512K blocks. However within a 32K block, mapping can also be performed downto a single byte resolution (useful for I/O mapping).

Selective Mapping of Memory Classes

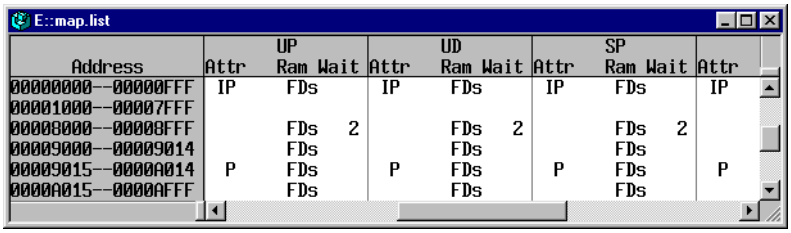


Address	UP Attr	UP Ram Wait	UD Attr	UD Ram Wait	SP Attr	SP Ram Wait	SD Attr	SD Ram Wait
00000000--00007FFF	I	FDs		FDs	I	FDs		FDs
00008000--000090FF	I	Ds	I	Ds	I	Ds	I	Ds
00009100--00009FFF		Ds		Ds		Ds		Ds
0000A000--0000A002			I	Ds			I	Ds
0000A003--0000AFFF				Ds				Ds

The address mapper can segment the memory into 4 segments. By using this segmentation, it is possible for example to split the memory so that a PROGRAM area can be mapped to the emulator RAM while the DATA area remains mapped as target memory. It is also possible to have totally separate physical memory areas displayed simultaneously.

Wait States and Write Protection

0 to 250 wait cycles can be specified within any particular address range.
Data access in specific address areas can be prevented. Using this feature for example, it is possible to prevent an I/O access occurring at a specific address (if bytewise mapping is operative).



Address	UP Attr	UP Ram Wait	UD Attr	UD Ram Wait	SP Attr	SP Ram Wait	Attr
00000000--00000FFF	IP	FDs	IP	FDs	IP	FDs	IP
00001000--00007FFF							
00008000--00008FFF		FDs 2		FDs 2		FDs 2	
00009000--00009014		FDs		FDs		FDs	
00009015--0000A014	P	FDs	P	FDs	P	FDs	P
0000A015--0000AFFF		FDs		FDs		FDs	

Support for External Bank Switching (up to 256 banks)

External bank switching schemes or MMUs can be supported by the memory mapper. For this there are separate probe inputs to the emulator. This option is only sensible on CPUs with less than 16 Mbyte addressing range.

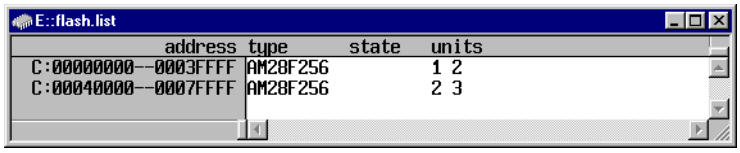
Support for EPROMs with Inbuilt Paging

EPROMs of the types 27513 or 27011 are supported without external logic. The address area within the EPROM has to be defined by the user, so that the emulator can support the device.

Support for Dynamic Memory in the Target System

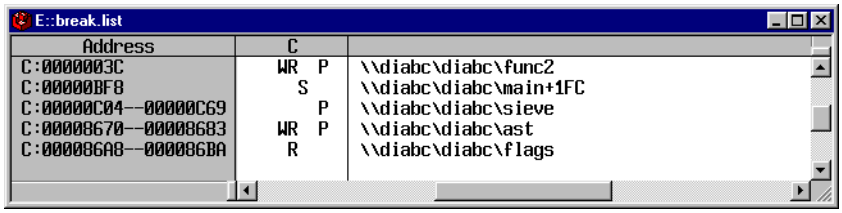
In order to refresh target dynamic RAM when the emulation is stopped, a memory refresh function is provided. The address range and memory class over which the refresh occurs can be defined.

Flash Programming



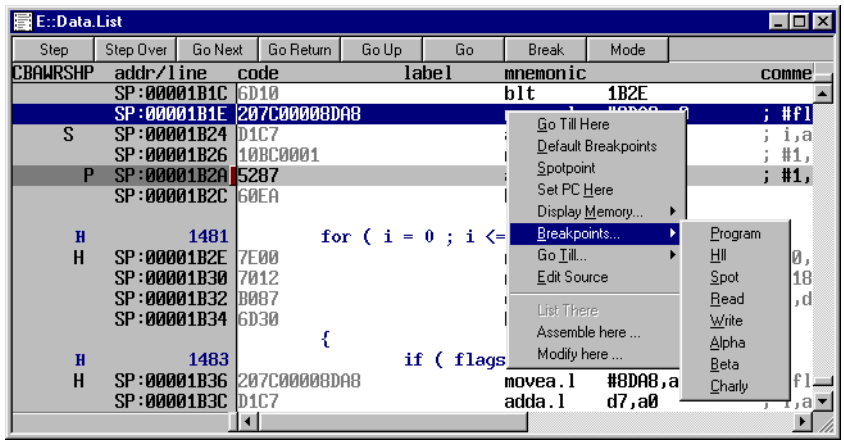
TRACE32 supports the programming of external flash memory as well as the programming of internal flash memory of microcontrollers. The programming can be controlled by the emulator or by a routine in the target system.

Memory Oriented Breakpoint System with up to 16 MByte Breakpoint Memory



Most currently available emulators use multiple address and data comparators to form the breakpoint system. This technique not only restricts the number of breakpoints available it also means that systems using bank selection are difficult to support. The breakpoint memory on the TRACE32 is basically a bytewide memory structure that can be mapped in a similar way like the overlay memory. When any memory location is accessed, the corresponding breakpoint byte is also accessed so that there are effectively 8 kinds of breakpoints for each addressable location.
The break memory is dual-ported, so that breakpoints can be set and displayed while the system is running.

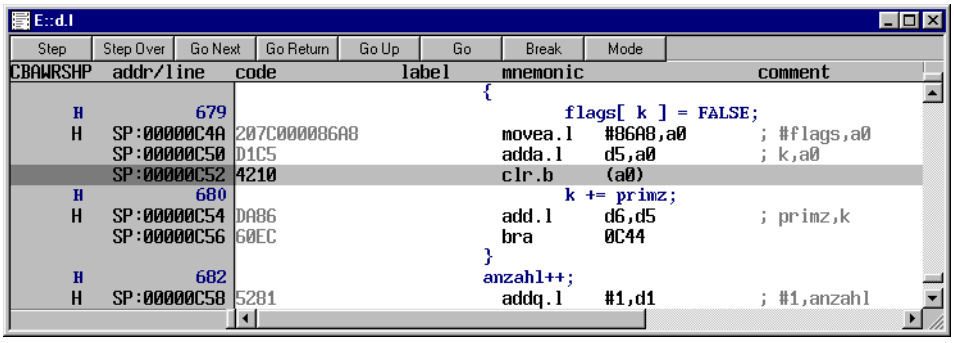
8 Breakpoint Types



- ❏ Program Breakpoint
- ❏ High-Level Breakpoint
- ❏ Spot Breakpoint
- ❏ Data Read Breakpoint
- ❏ Data Write Breakpoint
- ❏ General Purpose Point A
- ❏ General Purpose Point B
- ❏ General Purpose Point C

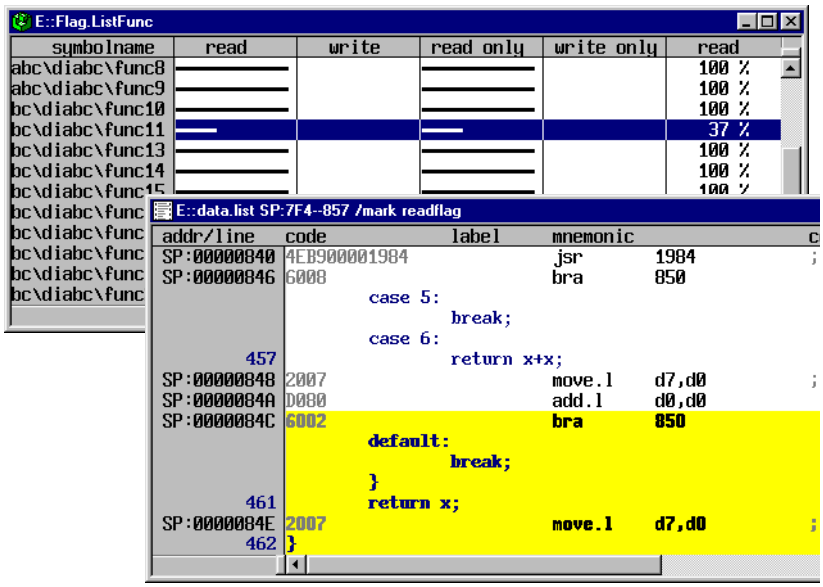
In each group there are up to 16 million breakpoints available depending upon the amount of breakpoint ram in the emulator. Breakpoints can be specified as a single address or an address range.

Hardware Support for High-Level Language Debugging



By using a specially reserved bit in the breakpoint memory, high-speed debugging of systems using high-level languages is available.

Flag System



Code Coverage

In a special memory, all addresses which are read or written are marked with read or write flags. This memory can therefore supply a lot of important information:

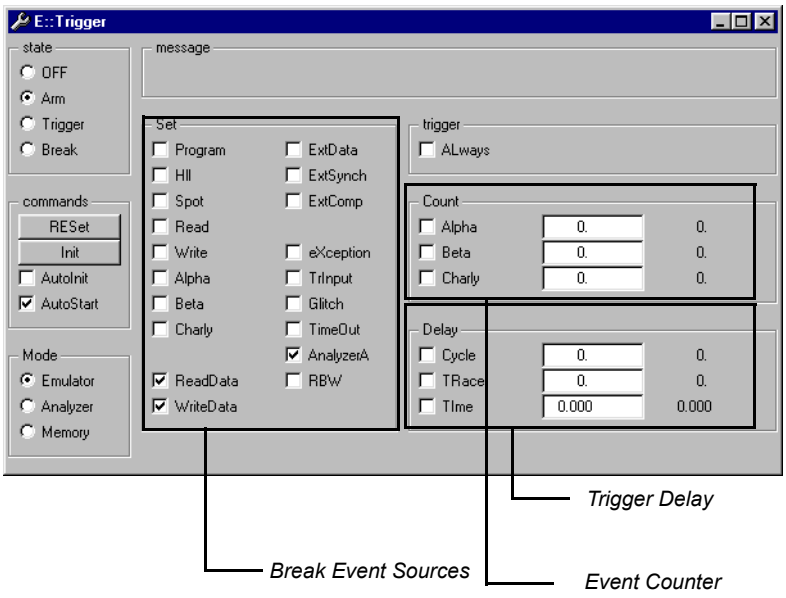
- ❏ Detection of uninitialised memory.
- ❏ Reading of uninitialised memory can be forced to generate an automatic break or to trigger the trace analyzer.
- ❏ Systematic program test due to the fact that each executed module will be marked in the flag ram.
- ❏ Detection of unused or unexecuted code.
- ❏ Systematic system test through visible code coverage analysis.
- ❏ Detecting accesses to unused or illegal address locations.

Trigger Outputs

8 trigger/status outputs are provided. These outputs are mainly intended for triggering or controlling certain functions within the target system. External analyzers can be triggered using the Trace Analyzer outputs.

- ❏ Emulator trigger output
- ❏ Emulator RUN and cycle signal
- ❏ Address signal from the breakpoint memory
- ❏ Pulse generator output
- ❏ Universal counter output

Break Event Sources



- ❏ Normal breakpoint
- ❏ High-level breakpoint
- ❏ Data read breakpoint
- ❏ Data write breakpoint
- ❏ General purpose breakpoint A
- ❏ General purpose breakpoint B
- ❏ General purpose breakpoint C
- ❏ Exception break (e.g. RESET, NMI etc.)
- ❏ Analyzer break A
- ❏ Bus timeout (TimeOut)
- ❏ Glitch Detector
- ❏ Synchronous external trigger event
- ❏ Asynchronous trigger event
- ❏ ReadBeforeWrite

Delayed Trigger

A trigger delay between the trigger event and the emulation break can be specified in terms of time, a cycle count or trace cycle count.

- ❏ Time delay 100ns to 300 days
- ❏ Cycles 0 to 2.8 E+14
- ❏ Trace cycles 0 to 2.8 E+14

The triggering can either stop the target CPU or only the recording in the trace buffer.

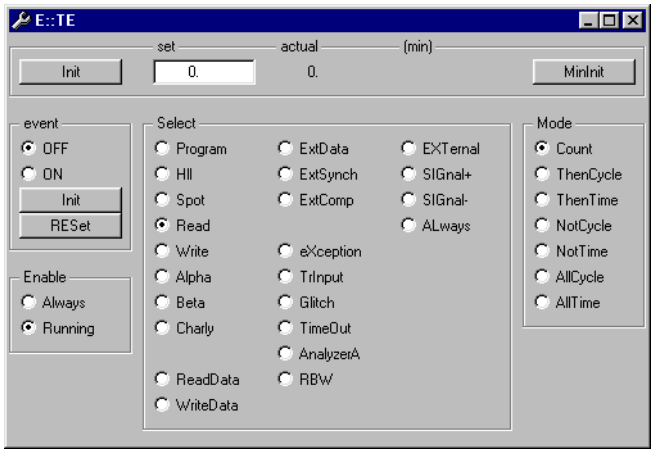
Event Counter

Each of the general purpose breakpoints A, B & C has an assosiated 48 bit counter. Using these counters it is possible to break not at the first, but at the nth trigger event.

Bus Timeout

A timeout for bus cycles to the target system can be defined. The cycle time can be within a range of 10µs to 10s. Expiry of the timeout period can be used to generate an emulator break.

Event Trigger



All trigger sources can also be selected as the source for the event trigger unit. The following trigger modes are posible:

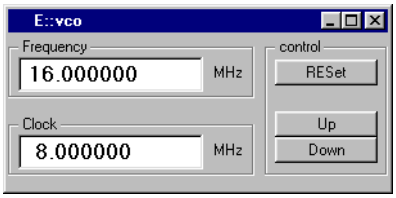
- ❏ Direct Trigger
- ❏ Trigger after N (1 .. 2.8E+14) cycles delay
- ❏ Trigger after T (100ns .. 300days) time delay
- ❏ Trigger after N events
- ❏ Delay trigger event fo N cycles
- ❏ Delay trigger event for T time
- ❏ Trigger if the specified trigger event does not happened within M (1 .. 65535) cycles
- ❏ Trigger if the specified trigger event does not happened within T time

Strobe Monitor for Target System

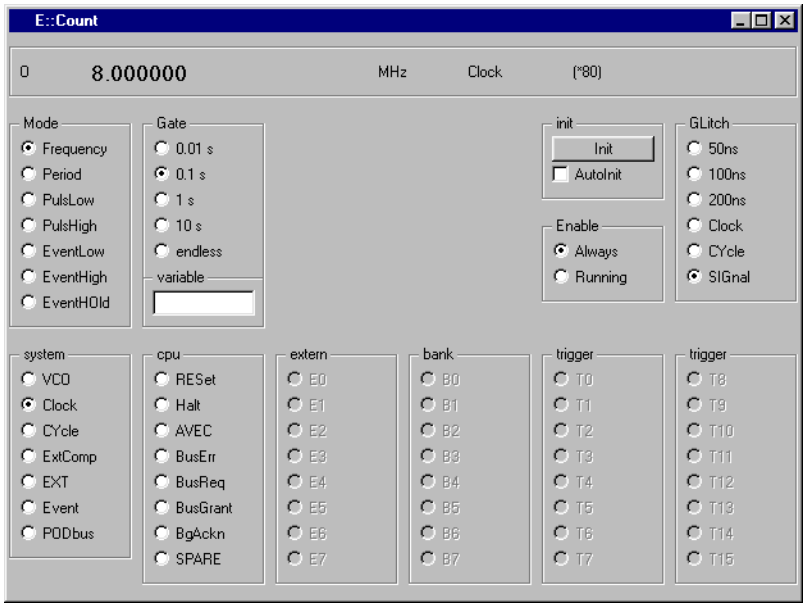
If the strobe period becomes >>10µs the system will alert the user. If programmed to do so, the emulator can go into a standby mode if this occurs .

Internal Frequency Generator

- Variable VCO with frequency range from 1 to 70 MHz.
- No phase change when frequency changed - this can be used to test the limiting frequencies of the target system. Output available for direct connection to the target system (BNC).
- Emulation CPU clock frequency programming is done via the emulation control unit.



Integrated Universal Counter



- Frequency 0 to 20MHz
- System clock 0 to 80MHz
- Pulse width 100ns to 300 days
- Positive or negative edge count
- 0 to 2.8E + 14
- Use for measuring of internal and external signals like cycle frequency, CPU clock frequency, interrupt frequency etc.

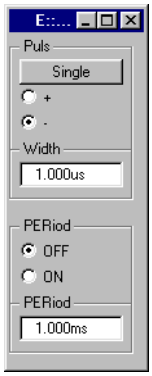
Inbuilt GLITCH-Detector for all important CPU signals

- Detection of glitches down to 5ns wide within a CPU cycle
- Break at glitch detection

Profiler

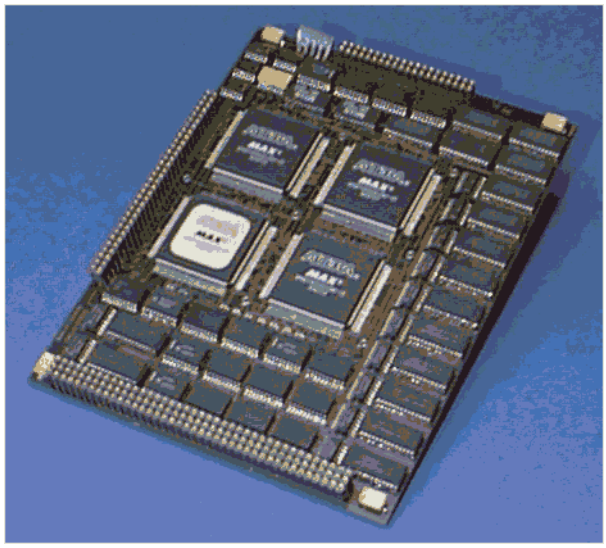
- ❏ Data transfer rates
- ❏ Interrupt rates
- ❏ System performance

Built-in Pulse Generator



- ❏ Pulse width 100ns to 6.5ms
- ❏ Single shot mode via keypress Break Monitor

State Analyzer HAC



The TRACE Analyzer HAC is designed as a high speed analyzer for CPU cycle times up to 50 ns. It is a part of the ECC32 and a cheap solution with reduced but sufficient trigger capabilites for most of the comon hardware and software designer demands. The analyzer offers a 32 Kbyte trace memory with a system synchronized time stamp unit and powerful and complex trigger capabilities. All important lines of the CPU are automatically connected to the analyzer. Universal input and output lines for trigger and stimulation can be connected via addtional probes. For more complex requirements, a HA120 can be mounted on the system without removeing the HAC.

88 Channel Trace

The HAC samples 88 bit per record. For 32 bit processors, additional trace buffer are located on the base modules. Up to 312 bit per record can therefore be controlled by the analyzer.

- 24 bit address
- 4 bit address range
- 16 bit data
- 8 bit state signals
- 4 bit bank access signals
- 16 bit universal channels
- 3 bit markers
- 3 bit 8 trigger levels
- 8 bit external trigger inputs
- 1 bit DMA access
- 4 bit task no.
- 8 bit reserved
- 5 bit internal

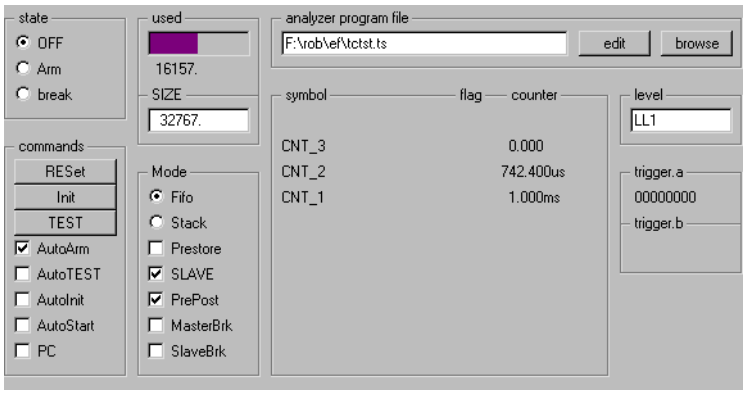
High-Speed down to 50ns Cycle Time

If necessary , CPU cycles up to 50 ns can be recorded. Also complex trigger input and output functions can be performed in 50 ns without touching real time program execution.

Large Trace Depth (32 KFrames)

The trace depth reaches 32 KFrames . This is much more than necessary , because of the flexible trigger unit, which allows exactly to specify the contents of the trace memory.

Operation Modes

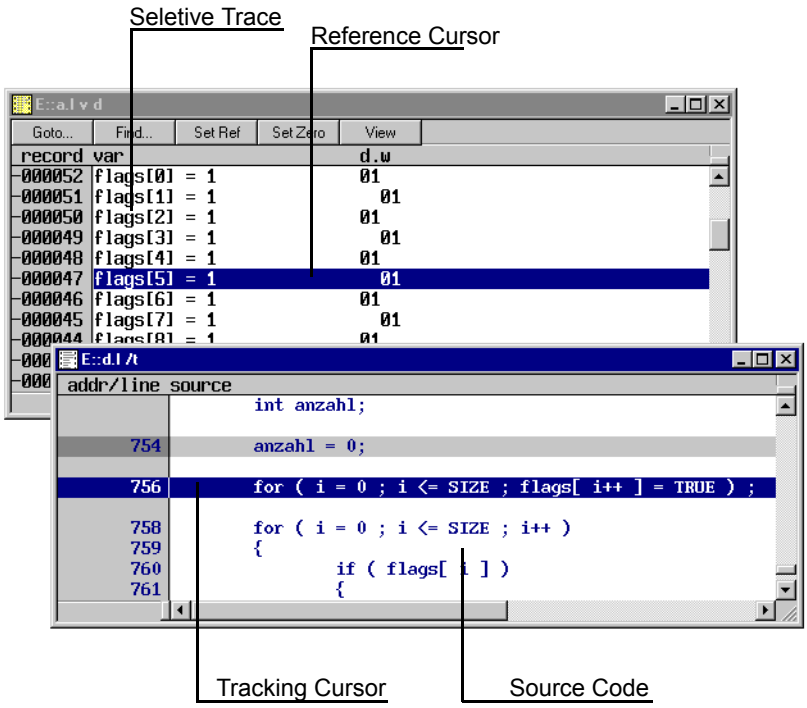


❏ FIFO mode
- records all until user program has been stopped.

❏ STACK mode
- records from program start until the trace memory is full.

PRESTORE Function

In the PRESTORE mode, the analyzer samples always an additional previous Opfetch cycle forced by hardware, if only data transfers should be sampled selected by the trigger unit.



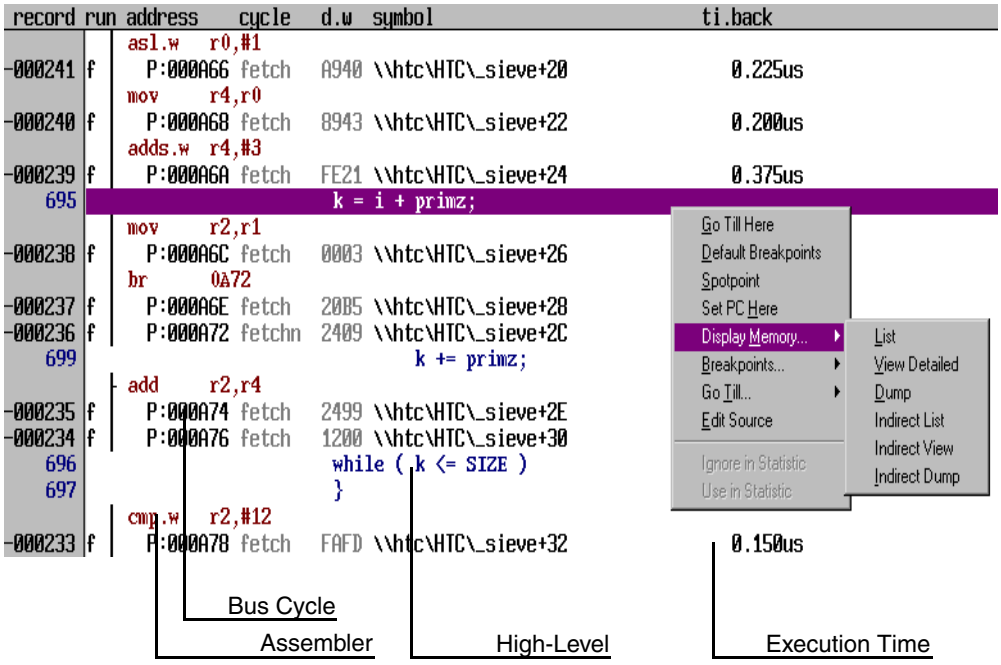
Internal Expansion Capability

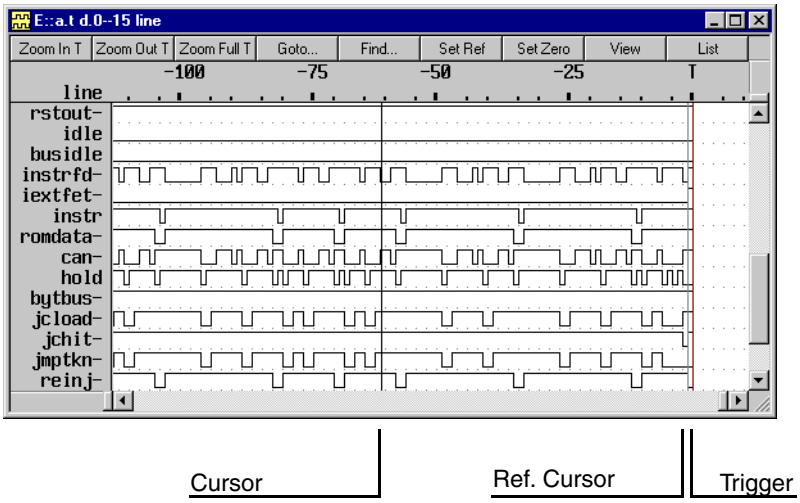
For emulator modules which need more trace capacity, the necessary extra bits are built into the emulator module itself (e.g. 64 additional channels with the trace board on microcontroller emulation heads).

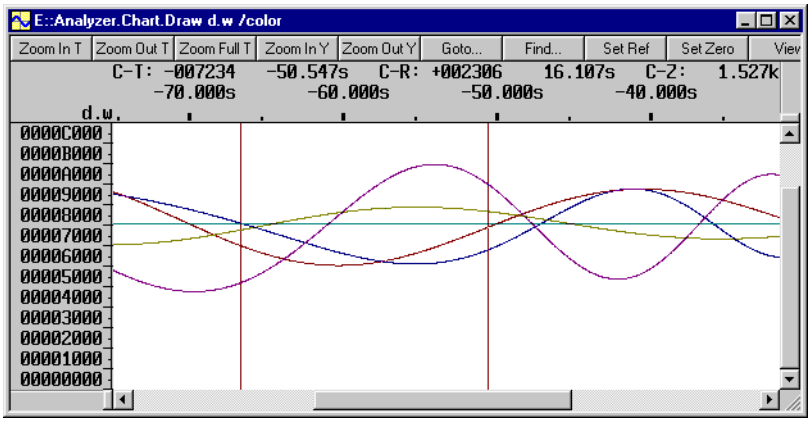
Various Trace Memory Display

- ❏ List
- ❏ Timing
- ❏ Chart
- ❏ Recordwise
- ❏ Assembler mnemonic
- ❏ Hex,binary,ASCII,etc.
- ❏ High Level Language
- ❏ Mixed language

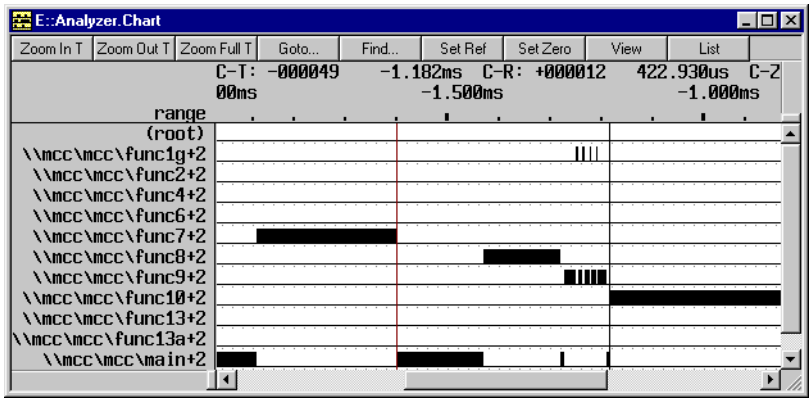
❑ Program source tracking



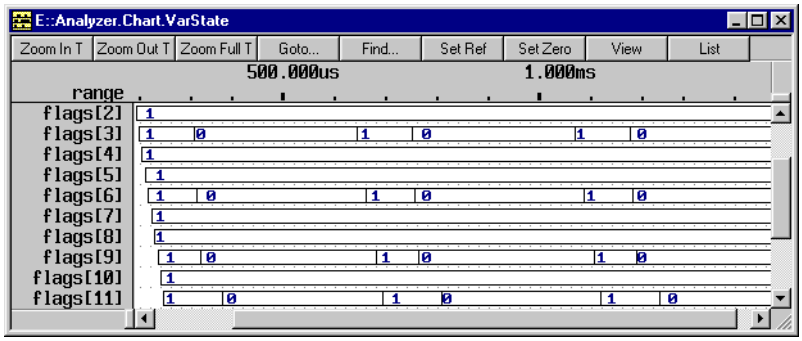




Graphical Display



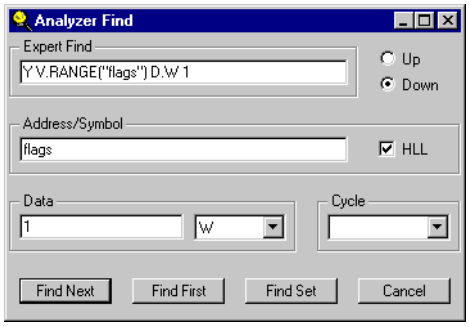
Execution Time Chart



Variable Time Chart

Powerful Trace Memory Manager

- ❏ Save memory
- ❏ Load memory
- ❏ Print memory
- ❏ Compare memory
- ❏ Find specific entry
- ❏ Goto record
- ❏ Time and record number evaluation.
- ❏ Referenz pointer
- ❏ User defined display

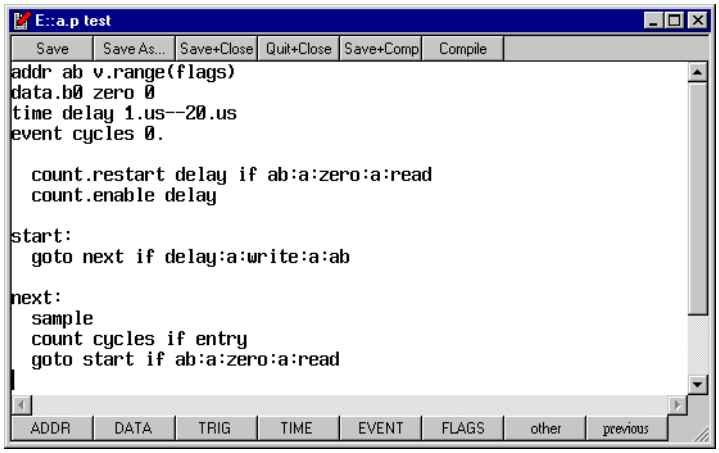


Analyzer Trigger Unit with 3 Levels

The level structure of the trigger unit allows quite flexible trigger combinations and sequences in consecutive and nonconsecutive order. Each level has the same priority and almost the same capabilities. A trigger program defines, under which circumstances a level can be reached or left, and therefore which trigger conditions or operations are the current or the next.

Analyzer Programming via a special Window

The programming of this complex trigger unit is done in an assembler like language for maximum flexibility. Using this language, the programming of very complex trigger sequences or operations can be defined. For simple demands, a pull down menu improves the programming for beginners.



Symbolic Operations for Analyzer Programming

All output operators and input variables can be entered in symbolic form. The target program symbols can also be used.

Trigger Sources

- ❏ Up to 2 address ranges
- ❏ Up to 2 data events (mask, range, ASCII, hex, binary)
- ❏ Up to 2*8 bit external trigger events
- ❏ CPU state (MEM READ, IO WRITE, INTA, ...)
- ❏ Counter outputs

External Trigger Inputs

- ❏ 1 inputs with 8 channels
- ❏ 1 trigger qualifiers for each trigger level
- ❏ Static levels of the trigger inputs can be read at any time
- ❏ Free format definition of external trigger events Hex and Mnemonic Display of Trace Data
- ❏

Trigger Operations

- ❏ Count.Enable
- ❏ Sample.Enable
- ❏ Trigger.Emulator
- ❏ Trigger.Exception
- ❏ Out (Target Stimulation)
- ❏ Break
- ❏ Spot
- ❏ GOTO level , CONTINUE

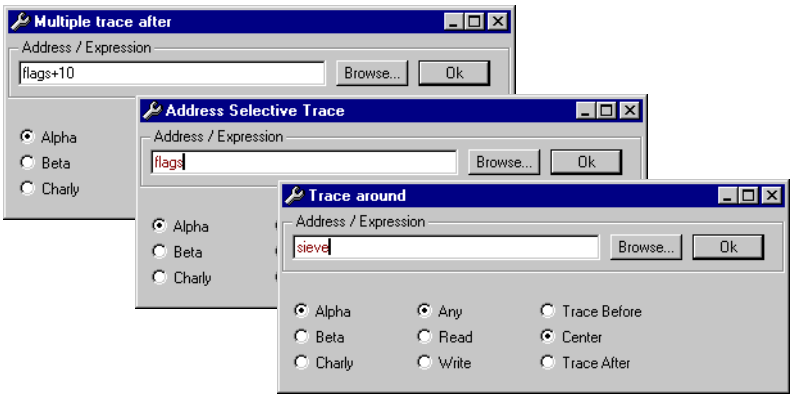
Free Format Definition of Data, Address and Trigger Events

- ❏ Hex and hex masks
- ❏ Binary and binary masks
- ❏ ASCII character and string
- ❏ Data ranges

Wizzards for Standard Trigger Problems

Time and Event Measurements with up to 3 Counters

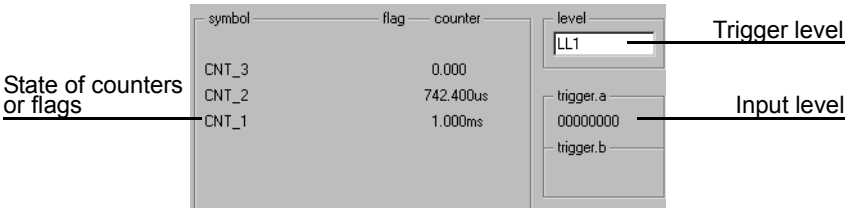
There are 2*16 bit counter for event measurement or event triggering and there is a 16 bit delay counter available. All counters are re-triggerable and can be evaluated as a part of an expression in the trigger sequences. Each counter can be used for timing measurements or as a counter for events.



- Event count 1 to 65536
- Cycles 1 to 65536
- Time 100ns resolutuion
- Retriggerable
- Selective release
- Trigger event when counter is zero
- Definition of time and event windows
- All Counters can be read `on the fly'

Trigger Monitor

A display of the counter values, the trigger values, the trigger levels and the trigger flags is available in the trigger monitor window.



Statistic Analyzer

- ❏ Time Stamp

  The Time Stamp Unit tags each trace record with a time value. These values are absolute and synchronized with all the other time values within the TRACE32 system.

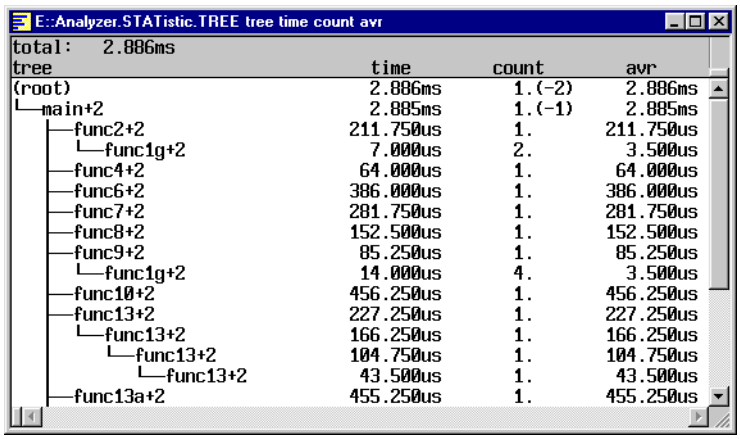
- ❏ Recording depth max. 32K
- ❏ 32 time stamp recording channels
- ❏ Resolution 100ns/1us

Function Analysis

- ❏ Min. and max. time
- ❏ Passes
- ❏ Include and exclude time

Link Analysis

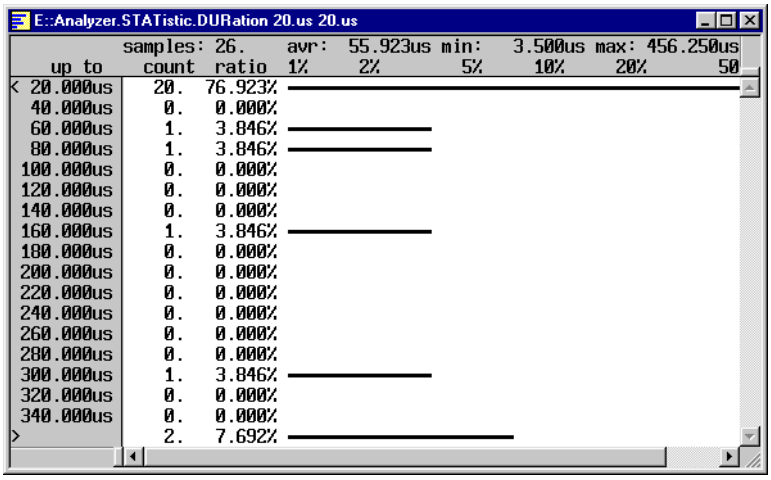
- ❏ Callers
- ❏ Min. and max. times
- ❏ Calls



Duration

- ❏ Execution time

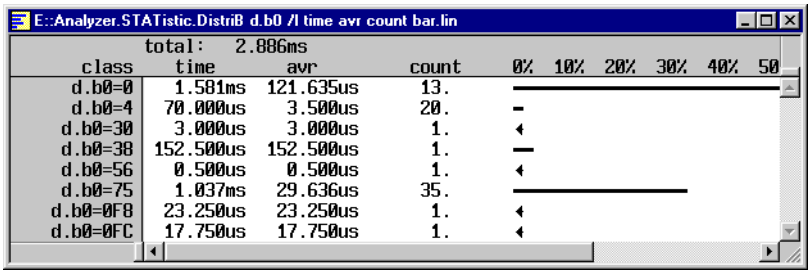
❑ Response time



Distance

❑ Time between samples

Distribution



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