

## Trace-based Debugging (CTS)

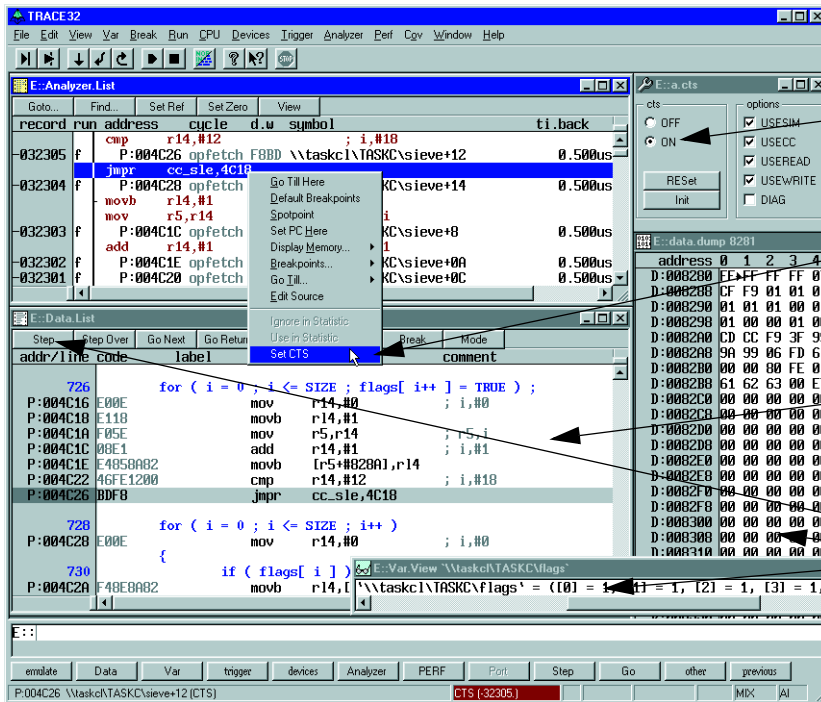
- Allows re-debugging of a traced program section
- Provides forward and backward debugging capabilities
- High-level language trace display including all local variables
- Timing and function nesting display
- Has the ability to fill most trace gaps caused by the limited bandwidth of trace port

In the past it was necessary to spend a lot of time analysing the trace listing in order to find out which instructions, data or system states had caused malfunctioning of the target system.

Now Trace-based Debugging - CTS for short - allows the user to recreate the state of the target system at a selected point based on the information sampled in the trace buffer. From this starting point the program steps previously recorded in real-time in the trace memory can be debugged again in TRACE32 PowerView GUI.



## Features



1.) Switch on the Context Tracking System

2.) Select the recording point for which the state of the target system is to be recreated

3.) The PC will be set automatically to the recording point

4.) During the trace-based debugging the changes of memories, variables and registers can be watched

### How does context tracking work?

After switching on the context tracking system you first select a recording point in the trace for which the target system state is to be recreated in the emulator. The program counter is then automatically set in the source listing to the point it was when the trace was recorded.

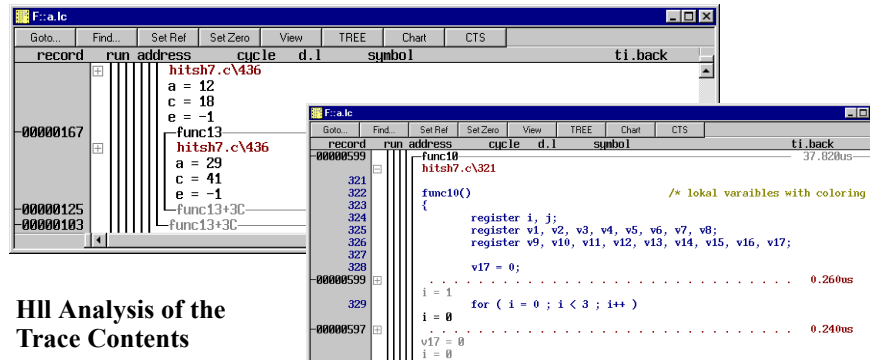
All debug commands such as Single Step, Step Over Call, Go Return, etc. can now be used. The CPU instructions are processed as they were recorded in the trace memory. The debug functionality has been further extended so that it is now also possible to step backwards.

At the same time it is also desirable to be able to track the changes of variables, memories and registers. There are various strategies available for this.

The changes can be followed relatively easily by using the write and read cycles recorded in the trace memory. However, this only functions for internal memories if the CPU shows complete information about these accesses.

Even then information about register transfers is not usually available. An exception to this is the C166 family which makes all information about internal operations visible externally via the bondout busses.

Another alternative is to use an instruction set simulator which effectively allows the individual instructions to be executed again. This enables registers and memory states to be recreated more easily. Instruction set simulators are available for PowerPC, 68K, 68HC05, 68HC08, 68HC11, 68HC12, 68HC16, SH2 and the ARM7.



**HLL Analysis of the Trace Contents**

```
record run address cycle d.l symbol ti.back
-00000167 hitsh7.c\436
a = 12
c = 18
e = -1
-00000125 func13
a = 29
c = 41
e = -1
-00000103 -func13+3C
-00000103 -func13+3C

record run address cycle d.l symbol ti.back
-00005599 func10 hitsh7.c\321 37.820us
321 hitsh7.c\321
322 func10() /* lokal variables with coloring
323 {
324 register i, j;
325 register v1, v2, v3, v4, v5, v6, v7, v8;
326 register v9, v10, v11, v12, v13, v14, v15, v16, v17;
327
328 v17 = 0;
-00005599 i = 1 ..... 0.260us
329 for ( i = 0 ; i < 3 ; i++ )
-00005597 i = 0 ..... 0.240us
v17 = 0
i = 0
```

## Contact

### International Representative

#### Argentina

Anacom Eletronica Ltda.  
Mr. Rafael Sorice  
Rua Nazareth, 807, Barcelona  
BR-09551-200 São Caetano do Sul, SP  
Phone: +55 11 3422 4200  
FAX: +55 11 3422 4242  
EMAIL: rsorice@anacom.com.br

#### Australia

Embedded Logic Solutions P/L  
Mr. Ramzi Kaffan  
Suite 2, Level 3  
144 Marsden Street  
Parramatta NSW 2150  
Phone: +61 2 9687 1880  
FAX: +61 2 9687 1881  
EMAIL: sales@emlogic.com.au

#### Austria

Lauterbach GmbH  
Altlaufstr. 40  
D-85635 Höhenkirchen-Siegertsbrunn  
Phone: +49 8102 9876 0  
FAX: +49 8102 9876 999  
EMAIL: info@lauterbach.com

#### Belgium

Tritec Benelux B.V.  
Mr. Robbert de Voogt  
Stationspark 550  
NL-3364 DA Slidrecht  
Phone: +31 184 41 41 31  
FAX: +31 184 42 36 11  
EMAIL: software@tritec.nl

#### Brazil

Anacom Eletronica Ltda.  
Mr. Rafael Sorice  
Rua Nazareth, 807, Barcelona  
BR-09551-200 São Caetano do Sul, SP  
Phone: +55 11 3422 4200  
FAX: +55 11 3422 4242  
EMAIL: rsorice@anacom.com.br

#### Canada

Lauterbach Inc.  
Mr. Udo Zoettler  
4 Mount Royal Ave.  
USA-Marlborough, MA 01752  
Phone: +1 508 303 6812  
FAX: +1 508 303 6813  
EMAIL: info\_us@lauterbach.com

#### China Beijing

Lauterbach Technologies Co., Ltd  
Mr. Linglin He  
Beijing Office  
A3, South Lishi Road, XiCheng District  
Beijing 100037, P.R. China  
Phone: +86 10 68023502  
FAX: +86 10 68023523  
EMAIL: linglin.he@lauterbach.com

#### China Shenzhen

Lauterbach Technologies Co., Ltd  
1406/E Xihaimingzhu Building  
No.1 Taoyuan Road, Nanshan District  
Shenzhen 518052, P.R. China  
Phone: +86 755 8621 0671  
FAX: +86 755 8621 0675  
EMAIL: emily.zhang@lauterbach.com

#### China Suzhou

Lauterbach Technologies Co., Ltd  
Mr. Linglin He  
Hengyu Square, Rm 709  
No. 188, Xing Hai Street  
Suzhou, 215021 P.R. of China  
Phone: +86 512 6265 8030  
FAX: +86 512 6265 8032  
EMAIL: info\_cn@lauterbach.com

#### Czech Republic

Lauterbach GmbH  
Altlaufstr. 40  
D-85635 Höhenkirchen-Siegertsbrunn  
Phone: +49 8102 9876 0  
FAX: +49 8102 9876 999  
EMAIL: info@lauterbach.com

#### Denmark

Nohau Danmark A/S  
Mr. Flemming Jensen  
Klausdalsbrovej 493  
DK-2730 Herlev  
Phone: +45 44 52 16 50  
FAX: +45 44 52 26 55  
EMAIL: info@nohau.dk

#### Egypt

Wantech Egypt  
Mr. Wagih A. Nawara  
5 Shafik Ghalie St., Suite 2  
Off Pyramids Road, Giza  
Cairo 12111  
Phone: +20 100 1251955  
FAX: +20 100 1250349  
EMAIL: sales@wantech.net.com

#### Finland

Nohau Solutions Finland  
Mr. Martti Viljainen  
Teknobulevardi 3-5  
FI-01531 Vantaa  
Phone: +358 40 546 1469  
FAX: +358 9 2517 8101  
EMAIL: sales@nohau.fi

#### France

Lauterbach S.A.R.L.  
Mr. Jean-Pierre Paradiso  
Europarc - Le Hameau B  
135 Chemin Des Bassins  
F-94035 Créteil Cedex  
Phone: +33 1 49 56 20 30  
FAX: +33 1 49 56 20 39  
EMAIL: info\_fr@lauterbach.com

#### Germany

Lauterbach GmbH  
Altlaufstr. 40  
D-85635 Höhenkirchen-Siegertsbrunn  
Phone: +49 8102 9876 0  
FAX: +49 8102 9876 999  
EMAIL: info@lauterbach.com

#### Germany North

Lauterbach GmbH  
Mr. Klaus Hommann  
Leonhardring 5  
D-31319 Sehnde  
Phone: +49 8102 9876 174  
FAX: +49 5138 6185 3  
EMAIL: klaus.hommann@lauterbach.com

**Germany South**

Lauterbach GmbH  
 Andreas Grimm  
 Altlaufstr. 40  
 D-85635 Höhenkirchen-Siegersbrunn  
 Phone: +49 8102 9876 190  
 FAX: +49 8102 9876 187  
 EMAIL: andreas.grimm@lauterbach.com

**Greece**

Lauterbach GmbH  
 Altlaufstr. 40  
 D-85635 Höhenkirchen-Siegersbrunn  
 Phone: +49 8102 9876 0  
 FAX: +49 8102 9876 999  
 EMAIL: info@lauterbach.com

**Hungary**

Lauterbach GmbH  
 Altlaufstr. 40  
 D-85635 Höhenkirchen-Siegersbrunn  
 Phone: +49 8102 9876 0  
 FAX: +49 8102 9876 999  
 EMAIL: info@lauterbach.com

**India-Bangalore**

Electro Systems Associates Pvt. Ltd.  
 Mr. G. V. Gurunatham  
 S-606, World Trade Center  
 Malleswaram West, No.26/1, Dr. Rajkumar  
 Road  
 India - Bangalore 560055  
 Phone: +91 80 67648888  
 FAX: +91 80 23475615  
 EMAIL: Trace32sales@esaindia.com

**India-Chennai**

Electro Systems Associates Pvt. Ltd.  
 Mr. D. Kannan  
 No.109/59A, Ground Floor  
 IV Avenue, Ashok Nagar  
 India - Chennai - 600 083 Tamilnadu  
 Phone: +91 044-24715750  
 FAX: +91 44 24715750  
 EMAIL: chennai@esaindia.com

**India-Delhi**

Electro Systems Associates Pvt. Ltd.  
 Mr. R.K. Bhandari  
 No. 705, 7th Floor, Laxmi Deep  
 Shivajinagar  
 India - Delhi - 110 092  
 Phone: +91 11-22549351  
 FAX:  
 EMAIL: delhi@esaindia.com

**India-Hyderabad**

Electro Systems Associates Pvt. Ltd.  
 Mr. C.V.M. Sri Ram Murthy  
 Shop No. 14, "Global Enclave"  
 Bhagyannagar Colony, Kukat pally  
 India - Hyderabad 500 072  
 Phone: +91 40-23063346  
 FAX: +91 40-23063346  
 EMAIL: hyderabad@esaindia.com

**India-Pune**

Electro Systems Associates Pvt. Ltd.  
 Mr. R K Bhandari  
 Shriram Complex, 1126/1, Model Colony  
 Shivajinagar  
 India - Pune - 411 016  
 Phone: +91 20 - 30462035 / 25663  
 FAX: +91 20-25677202  
 EMAIL: pune@esaindia.com

**Ireland**

Lauterbach Ltd.  
 Mr. Barry Lock  
 11 Basepoint Enterprise Centre  
 Stroudley Road  
 Basingstoke, Hants RG24 8UP  
 Phone: +44-1256-333-690  
 FAX: +44-1256-336-661  
 EMAIL: info\_uk@lauterbach.com

**Israel**

Itec Ltd.  
 Mr. Mauri Gottlieb  
 P.O. Box 10002  
 IL-Tel Aviv 61100  
 Phone: +972 3 6491202  
 FAX: +972 3 6497661  
 EMAIL: general@itec.co.il

**Italy**

Lauterbach Srl  
 Mr. Maurizio Menegotto  
 Via Enzo Ferrieri 12  
 I-20153 Milano  
 Phone: +39 02 45490282  
 FAX: +39 02 45490428  
 EMAIL: info\_it@lauterbach.com

**Japan**

Lauterbach Japan, Ltd.  
 Mr. Kenji Furukawa  
 3-8-8 Shinyokohama  
 Kouhoku-ku, Nisso 16th Building  
 Yokohama-shi, Japan 222-0033  
 Phone: +81 45 477 4511  
 FAX: +81 45 477 4519  
 EMAIL: info@lauterbach.co.jp

**Luxembourg**

Tritec Benelux B.V.  
 Mr. Robbert de Voogt  
 Stationspark 550  
 NL-3364 DA Sliedrecht  
 Phone: +31 184 41 41 31  
 FAX: +31 184 42 36 11  
 EMAIL: software@tritec.nl

**Malaysia**

Flash Technology  
 Mr. Teo Kian Hock  
 No 61, # 04-15 Kaki Bukit Av 1  
 Shun Li Industrial Park  
 SGP-Singapore 417943  
 Phone: +65 6749 6168  
 FAX: +65 6749 6138  
 EMAIL: teokh@flashtech.com.sg

**Mexico**

Lauterbach Inc.  
 Mr. Udo Zoettler  
 4 Mount Royal Ave.  
 USA-Marlborough, MA 01752  
 Phone: +1 508 303 6812  
 FAX: +1 508 303 6813  
 EMAIL: info\_us@lauterbach.com

**Netherlands**

Tritec Benelux B.V.  
 Mr. Robbert de Voogt  
 Stationspark 550  
 NL-3364 DA Sliedrecht  
 Phone: +31 184 41 41 31  
 FAX: +31 184 42 36 11  
 EMAIL: software@tritec.nl

**New Zealand**

Embedded Logic Solutions P/L  
 Mr. Ramzi Kattan  
 Suite 2, Level 3  
 144 Marsden Street  
 Parramatta NSW 2150  
 Phone: +61 2 9687 1880  
 FAX: +61 2 9687 1881  
 EMAIL: sales@emlogic.com.au

**Norway**

Nohau Solutions AB  
 Mr. Jörgen Nilsson  
 Derbyvägen 4  
 SE-21235 Malmö  
 Phone: +46 40 592 206  
 FAX: +46 40 592 229  
 EMAIL: sales@nohau.se

**Poland**

QUANTUM Sp. z o.o.  
 Mr. Aleksander Bil  
 ul. Jeleniogorska 6  
 54-056 Wrocław  
 Phone: +48 71 362 6356  
 FAX: +48 71 362 6357  
 EMAIL: info@quantum.com.pl

**Portugal**

Captura Electronica, SCCL  
Mr. Juan Martinez  
c/Duero, 40  
E-08031 Barcelona  
Phone: +34 93 429 5730  
FAX: +34 93 407 0778  
EMAIL: info@captura-el.com

**Romania**

Lauterbach GmbH  
Altlaufstr. 40  
D-85635 Höhenkirchen-Siegersbrunn  
Phone: +49 8102 9876 0  
FAX: +49 8102 9876 999  
EMAIL: info@lauterbach.com

**Russia**

RTSoft  
Mr. Alexey Isaev  
Nikitinskaya 3  
RUS-105037 Moscow  
Phone: +7 495 742 6828  
FAX: +7 495 742 6829  
EMAIL: sales@rtsoft.msk.ru

**Singapore**

Flash Technology  
Mr. Teo Kian Hock  
No 61, # 04-15 Kaki Bukit Av 1  
Shun Li Industrial Park  
SGP-Singapore 417943  
Phone: +65 6749 6168  
FAX: +65 6749 6138  
EMAIL: teokh@flashtech.com.sg

**South Korea, Pangyo**

MDS Technology Co., Ltd.  
Mr. Sangheon Lee  
3FL, Hancom Tower  
49, Daewangpangyo-ro 644, Bundang-gu  
Seongnam-si, Gyeonggi-do, 463-400, ROK  
Phone: +82-31-627-3000  
FAX: +82-31-627-3100  
EMAIL: trace32@mdstec.com

**Spain**

Captura Electronica, SCCL  
Mr. Juan Martinez  
c/Duero, 40  
E-08031 Barcelona  
Phone: +34 93 429 5730  
FAX: +34 93 407 0778  
EMAIL: info@captura-el.com

**Sweden**

Nohau Solutions AB  
Mr. Jörgen Nilsson  
Derbyvägen 4  
SE-21235 Malmö  
Phone: +46 40 592 206  
FAX: +46 40 592 229  
EMAIL: sales@nohau.se

**Switzerland**

JDT Jberg DatenTechnik  
Mr. Andreas Jberg  
Zimmereistrasse 2  
CH-5734 Reinach AG  
Phone: +41 62 7710 886  
FAX:  
EMAIL: Andreas.Jberg@jdt.ch

**Taiwan**

Superlink Technology Corp.  
Mr. Sulin Huang  
3F-8, No. 77, Sec. 1, Xintaiwu Rd., Xizhi District,  
New Taipei City 22101, Taiwan, R.O.C.  
Phone: +886 2 26983456  
FAX: +886 2 26983535  
EMAIL: info.stc@superlink.com.tw

**Tunisia**

Lauterbach Consulting S.A.R.L.  
Mr. Khaled Jmal  
Route El Ain Km 3.5  
TN-3062 Sfax  
Phone: +216-74611730  
FAX: +216-74611723  
EMAIL: info\_tn@lauterbach.com

**Turkey-1**

Tektronik Muh. ve Tic. A.S.  
Mr. Hakan Yavuz  
CyberPlaza B-Blok, 702B  
Bilkent  
06800 Ankara  
Phone: +90 312 437 3000  
FAX: +90 312 437 1616  
EMAIL: info@tektronik.com.tr

**Turkey-2**

G3TEK Embedded Technologies Ltd.  
Mr. Celal Aygun  
Ilkyerlesim Mah. 445.  
Sok. No: 48  
06370 Batikent/Ankara  
Phone: +90 312 3324769  
FAX: +90 312 3324769  
EMAIL: info@g3tek.com

**UK**

Lauterbach Ltd.  
Mr. Barry Lock  
11 Basepoint Enterprise Centre  
Stroudley Rd  
Basingstoke, Hants RG24 8UP  
Phone: +44 1256 333 690  
FAX: +44 1256 350 301  
EMAIL: info\_uk@lauterbach.com

**USA East**

Lauterbach Inc.  
Mr. Udo Zoettler  
4 Mount Royal Ave.  
USA-Marlborough, MA 01752  
Phone: +1 508 303 6812  
FAX: +1 508 303 6813  
EMAIL: info\_us@lauterbach.com

**USA West**

Lauterbach Inc.  
Mr. Bob Kupyń  
1111 Main Street, Suite 620  
USA-Vancouver, WA, 98660  
Phone: +1 503 524 2222  
FAX: +1 503 524 2223  
EMAIL: bob.kupyń@lauterbach.com

---

## Additional Information

<http://www.lauterbach.com>

### Lauterbach GmbH

Altlaufstr. 40  
D-85635 Höhenkirchen-Siegertsbrunn  
Tel. ++49 8102 9876-0 FAX -999  
info@lauterbach.com  
http://www.lauterbach.de

### Lauterbach Inc.

4 Mount Royal Ave.  
Marlboro MA 01752  
Phone (508) 303 6812 FAX (508) 303 6813  
info\_us@lauterbach.com  
http://www.us.lauterbach.com

### Lauterbach Ltd.

11 Basepoint Enterprise Ctre Stroudley Road  
Basingstoke, Hants RG24 8UP  
Phone ++44-1256-333-690 FAX -661  
info\_uk@lauterbach.com  
http://www.lauterbach.co.uk

### Lauterbach S.A.R.L.

135 Chemin Des Bassins  
F-94035 Créteil Cedex  
Phone ++33-149-562-030  
FAX ++33-149-562-039  
info\_fr@lauterbach.com  
http://www.lauterbach.fr

### Lauterbach Japan, Ltd.

3-9-5 Shinyokohama Kouhoku-ku  
Yokohama-shi Japan 222-0033  
Phone ++81-45-477-4511 FAX -4519  
info\_j@lauterbach.com  
http://www.lauterbach.co.jp

### Lauterbach s.r.l.

Lauterbach s.r.l.  
Via Enzo Ferrieri 12  
I-20153 Milano  
Phone ++39 02 45490282  
FAX ++39 02 45490428  
info\_it@lauterbach.it  
http://www.lauterbach.it

### Suzhou Lauterbach Consulting Co.,Ltd.

Room 1605, Xing Hai International Square  
No.200, Xing Hai Street  
Suzhou, 215021 PR of China  
Phone: 0086-512 6265 8030  
FAX: 0086-512 6265 8032  
info\_cn@lauterbach.cn  
http://www.lauterbach.cn

---

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