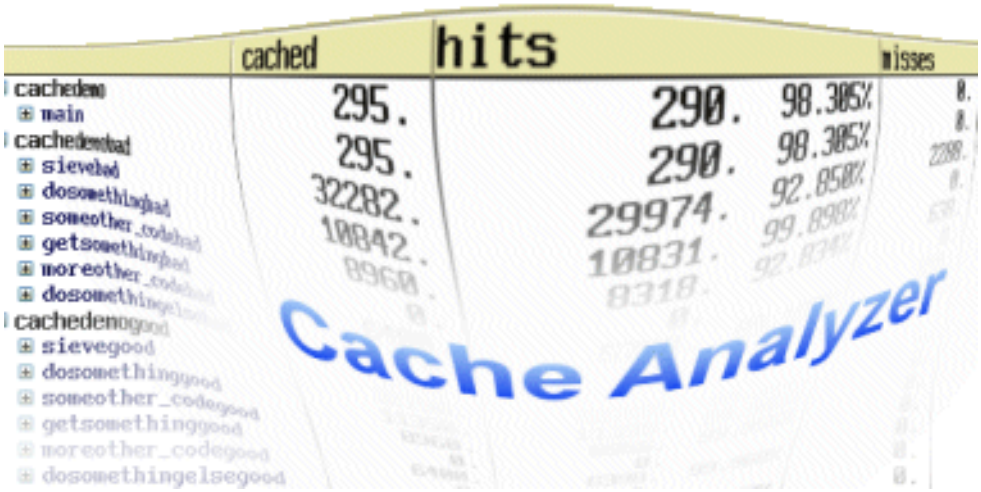
TRACE32®
Technical Information

Cache Analyzer



Cache Analyzer

embedded AWARD 2005

- Basic support for all microcontrollers
- Advanced support for ARM architecture
- Optimize instruction and data cache usage
- Find bus transfer bottlenecks
- Verify effects of code optimisation
- Simulate effects of different cache sizes
- Various graphical and numerical displays

The cache analysis tool provides developers of embedded systems with the following benefits:

1) Optimization of program run times

2) Reduction in power consumption of the entire system

Cache analysis can be performed on all microcontrollers, cache architectures, and cache hierarchies. If required, the predefined cache structure of microcontrollers can also be modified. In this way, an alternative cache structure can be tested to

determine if its use will lead to greater cache efficiency and therefore shorten program run times. The result can then be taken into account for future designs.

LAUTERBACH DEVELOPMENT TOOLS

Cache Analyzer

Overview

Microcontrollers that operate at rates of more than 200 MHz can only achieve optimum program run times in embedded systems if their caches are used efficiently. This article describes how the TRACE32-PowerTrace microprocessor development tool is used to analyze the relationship between cache efficiency and program run times.

Introduction

A cache is a small, fast memory that is generally integrated directly in the microcontroller. Individual program parts are temporarily stored in the cache so that the microcontroller does not have to retrieve each program instruction or data item from the slow external memory. However, the cache can only store a limited number of program instructions or data items required because of its small size (128 KB to 1 MB). As a result, various parts of the program compete for space in the cache and evict each other. The cache structure determines which program parts compete for a place in the cache and constantly replace other program parts.

Cache Addressing

Short sections of program (usually 16 or 32 bytes) can be temporarily stored in a cache line to enable quick access. Cache addressing, which is defined by the cache structure, determines in which cache line the instructions and data items of individual memory addresses are stored. As the memory address mapping on the cache line provides the basis for analyzing cache efficiency, it is necessary to understand the process of cache addressing.

Cache addressing uses the memory address to determine in which cache line the required program part is to be temporarily stored. The analyses discussed in this article use a 2-way set associative cache. In a 2-way set associative cache two cache lines are allowed to hold the instructions or data of a memory address.

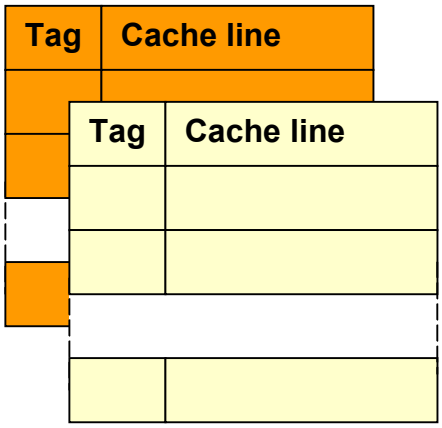


Figure 1: Diagram of a 2-way associative cache

The given example of a cache has the following data:

- 16 bytes per cache line
- 512 cache lines

Using this data, a 32-bit memory is mapped as follows to a cache line:

- **Bits [3..0]** are used to determine the address of the word/byte within the cache line (4 bits for 16 bytes per cache line)
- **Bits [12..4]** are used to select the cache line (9 bits for 512 cache lines)
- **Bits [31..13]** are entered as the tag in the cache line. The bits [31..13] of a memory address are compared with the tag to determine whether a program instruction or data item is already stored in a cache line.

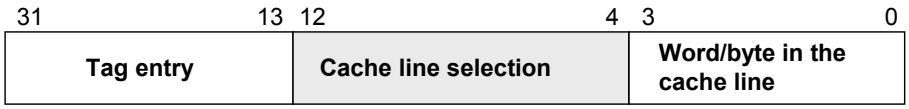


Figure 2: In the example of a cache, the bits [12..4] of the memory address determine in which cache line the program instructions/data items are to be temporarily stored.

This type of cache addressing means

line 0x15:

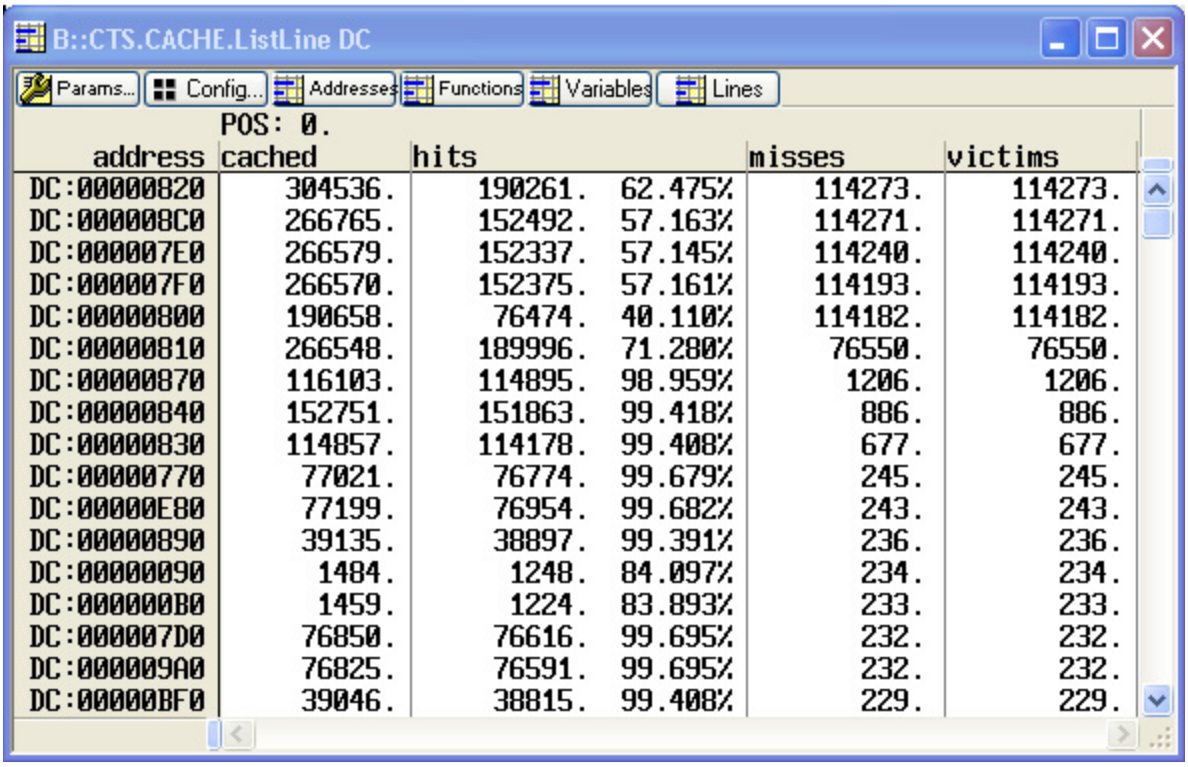
```
0x8150:  0000 0000 0000 0000
100 0   0001 0101 0000
0xA150:  0000 0000 0000 0000
101 0   0001 0101 0000
```

```
0xC150:  0000 0000 0000 0000
110 0  0001 0101 0000
```

If three or more addresses compete for the same cache line in a 2-way associative cache, the memory contents of the address are repeatedly evicted from the cache. When an entry is replaced, the evicted cache contents have to be reloaded into the cache when the program requires them again. The contents have to be accessed from the external memory each time. This is to be avoided if possible for the following reasons:

- Current access times for external memories show that the rate at which an instruction or data item is retrieved from the external memory, is on average, 10 to 30 times slower than when the data is stored in the cache. Each time the external memory is accessed, the program execution time slows down considerably.
- Each time the external memory is accessed, the power consumption of the entire system increases immediately by a significant level . This is a great disadvantage for portable, battery-powered devices.

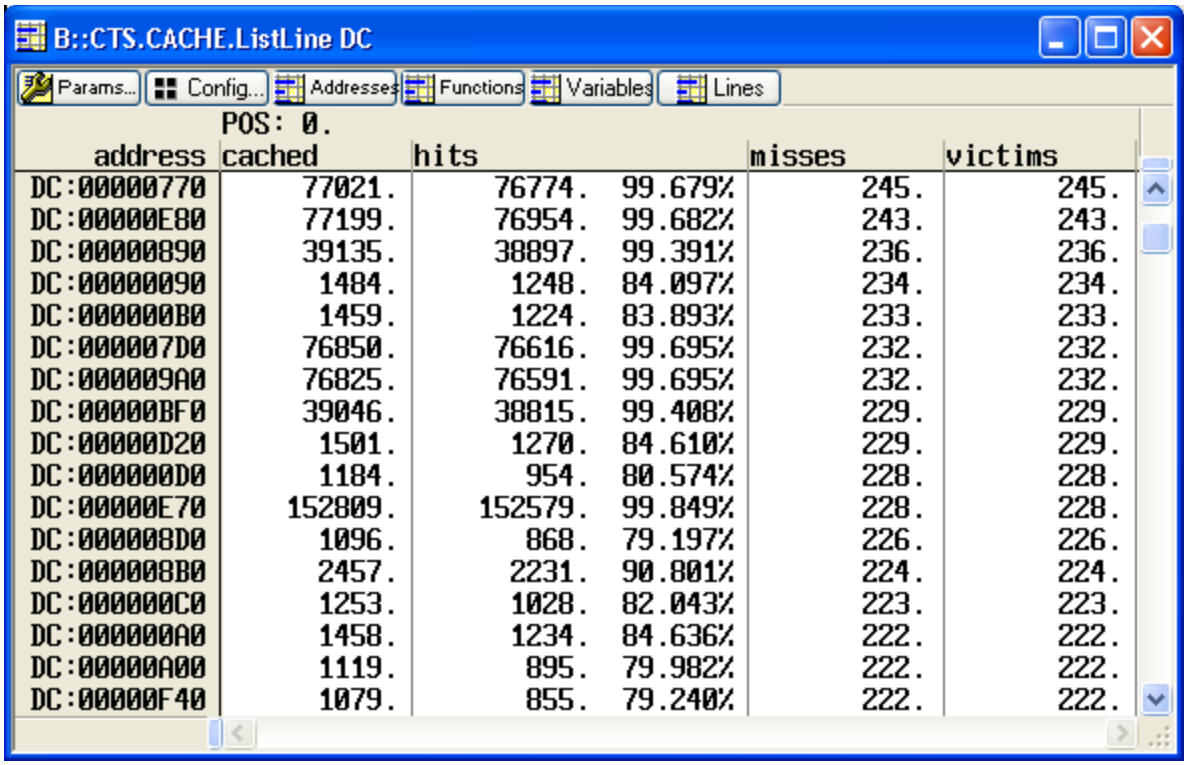
The best way to reduce the frequency with which the external memory is accessed, is to prevent unnecessary eviction from the cache. Unnecessary eviction always occurs when several memory addresses compete for a limited number of cache lines, while other cache lines are hardly being used, if at all.



address	cached	hits		misses	victims
DC:00000820	304536.	190261.	62.475%	114273.	114273.
DC:000008C0	266765.	152492.	57.163%	114271.	114271.
DC:000007E0	266579.	152337.	57.145%	114240.	114240.
DC:000007F0	266570.	152375.	57.161%	114193.	114193.
DC:00000800	190658.	76474.	40.110%	114182.	114182.
DC:00000810	266548.	189996.	71.280%	76550.	76550.
DC:00000870	116103.	114895.	98.959%	1206.	1206.
DC:00000840	152751.	151863.	99.418%	886.	886.
DC:00000830	114857.	114178.	99.408%	677.	677.
DC:00000770	77021.	76774.	99.679%	245.	245.
DC:00000E80	77199.	76954.	99.682%	243.	243.
DC:00000890	39135.	38897.	99.391%	236.	236.
DC:00000090	1484.	1248.	84.097%	234.	234.
DC:000000B0	1459.	1224.	83.893%	233.	233.
DC:000007D0	76850.	76616.	99.695%	232.	232.
DC:000009A0	76825.	76591.	99.695%	232.	232.
DC:00000BF0	39046.	38815.	99.408%	229.	229.

Figure 3: Several memory addresses compete for a limited number of cache lines, while other cache lines are hardly used.

Cache efficiency can be optimized by modifying the relocation information in the linker command file so that functions and data are placed in the memory in such a way that competition for cache lines is distributed as evenly as possible.



POS: 0.

address	cached	hits		misses	victims
DC:00000770	77021.	76774.	99.679%	245.	245.
DC:00000E80	77199.	76954.	99.682%	243.	243.
DC:00000890	39135.	38897.	99.391%	236.	236.
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DC:000007D0	76850.	76616.	99.695%	232.	232.
DC:000009A0	76825.	76591.	99.695%	232.	232.
DC:00000BF0	39046.	38815.	99.408%	229.	229.
DC:00000D20	1501.	1270.	84.610%	229.	229.
DC:000000D0	1184.	954.	80.574%	228.	228.
DC:00000E70	152809.	152579.	99.849%	228.	228.
DC:000008D0	1096.	868.	79.197%	226.	226.
DC:000008B0	2457.	2231.	90.801%	224.	224.
DC:000000C0	1253.	1028.	82.043%	223.	223.
DC:000000A0	1458.	1234.	84.636%	222.	222.
DC:00000A00	1119.	895.	79.982%	222.	222.
DC:00000F40	1079.	855.	79.240%	222.	222.

Figure 4: Competition for cache lines is distributed evenly.

Before developers of embedded designs can optimize the positioning of functions and data in the memory, they require an analysis tool that can trace any unnecessary eviction from the cache. Since October 2004, Lauterbach Datentechnik GmbH has provided a cache analysis tool for its TRACE32-PowerTrace microprocessor development system.

Cache Analysis

Before describing how to carry out a cache analysis, here is a short definition of some important terms:

- **Cache hit:** An instruction or data item required by the program that is located in the cache.
- **Cache miss:** An instruction or data item required by the program that is not located in the cache and therefore has to be loaded from the external memory.
- **Cache victim:** An instruction or data item evicted from the cache, in order to create a cache miss place for the program part currently required.

The following steps are required to carry out a cache analysis using TRACE32-PowerTrace for a selected system function (for example, image compression for a cellular telephone):

Identifying the cache structure

The TRACE32 software identifies the cache structure of the microcontroller used in the target system. The instruction cache (IC) has the same cache structure as the cache structure described in the introduction.

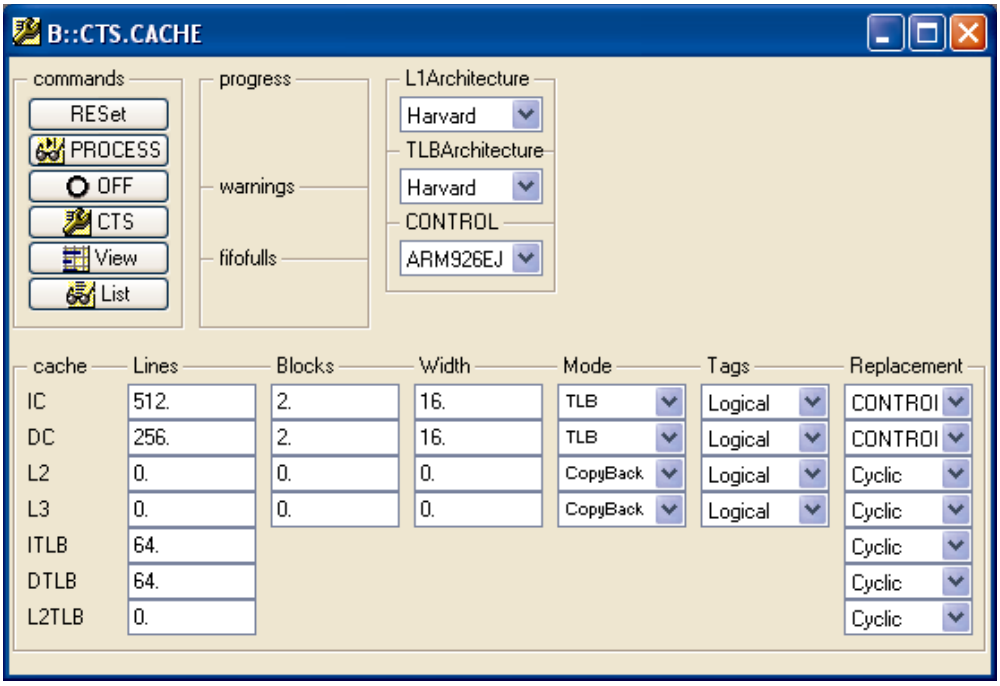

Figure 5: Automatic definition of the cache structure of the microcontroller

The software can identify all cache structures and cache hierarchies currently available on the market, including level 2/level 3 caches. TRACE32 also supports cache structures that have been configured using a memory protection unit (MPU) or a memory management unit (MMU).

Recording program and data flow in the trace memory

Cache analysis is based on the program and data flow recorded in the trace memory. TRACE32-PowerTrace provides a 128-MFrame trace memory, which can record up to 10 seconds of program run time.

Evaluating the results of the analysis

Cache analysis determines the cache hit, cache miss, and cache victim rates for the recorded program and data flow based on the defined cache structure. To avoid unnecessary eviction from the cache, the following information is required:

- ❏ Which cache lines have a particularly high cache victim rate?
- ❏ Which parts of the program are competing for these lines?
- ❏ Are there any cache lines that are not, or hardly, being used?

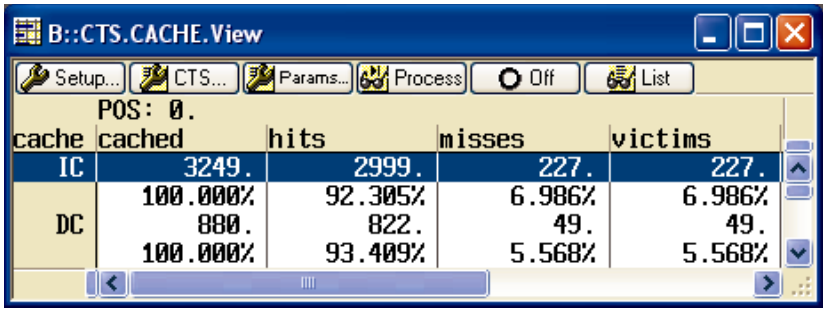

Figure 6: Analysis of the cache hit/cache miss/cache victim rates fo instruction cache (IC) and data (DC) caches

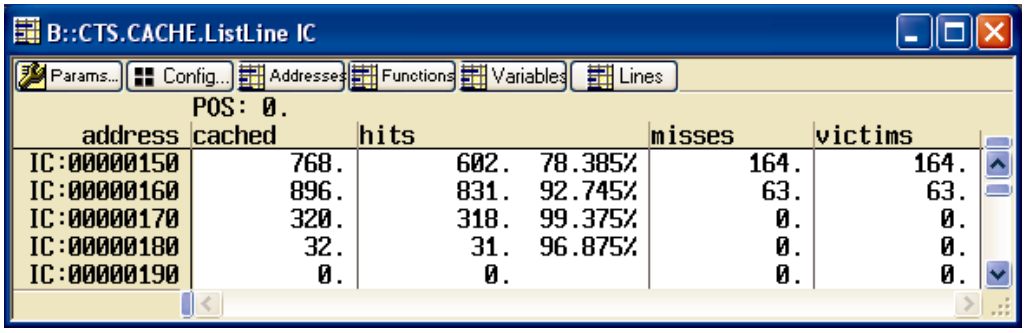

Figure 7: Analysis of the cache hit/cache miss/cache victim rates for the individual cache lines of the instruction cache

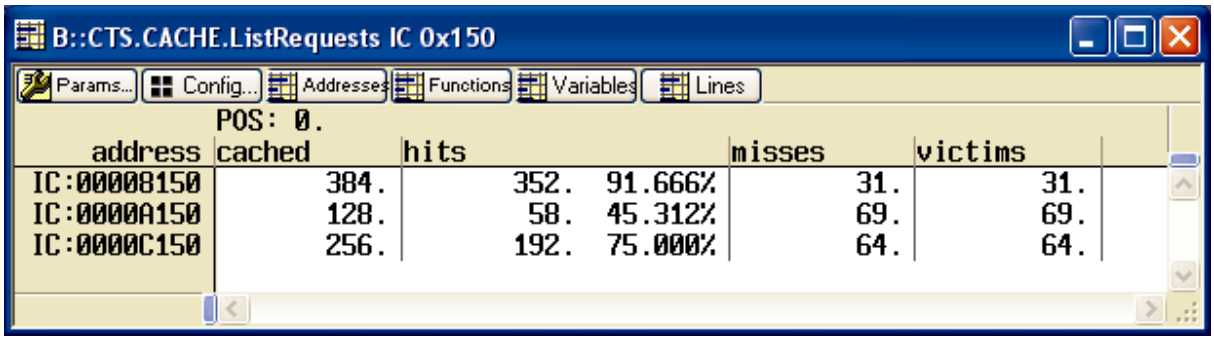

Figure 8: List of program addresses competing for cache line 0x15 of the instruction cache

Figure 8 in the above analysis shows that the program instructions at the addresses, 0x8**15**0, 0xA**15**0, and 0xC**15**0, are competing for the cache line 0x15. The above example uses a cache in which each cache line has two locations in the cache (2-way associative cache). Three program addresses are competing for one cache line; therefore, eviction will always occur, resulting in cache victims. At the same time, cache line 0x19 is completely unused. By redirecting the address of one of the competing program instructions to the end address 0x190, the competition can be removed from cache line 0x15 and there will be no further cache victims.

Relationship Between Cache Efficiency and Program Run Time

As described in the previous section, cache analysis is based on the program and data flow recorded in the trace memory. As all entries in the trace memory have a time stamp, the trace contents are used as the basis for run time measurements. This has the advantage that the direct relationship between program run time and cache efficiency can be measured and verified using TRACE32-PowerTrace.

Figure 9 shows how the function analyzed has a cache hit rate of 79% and a cache victim rate of 21% for the cache line 0x15.

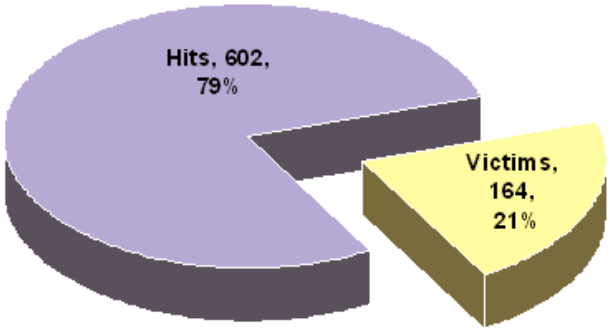

Figure 9: Graphical analysis of the cache hit/cache victim rates for the cache line 0x15.

The high rate of replacement also becomes apparent when the function's run time is studied. The average run time of the function (sievebad) is 77.6 us.

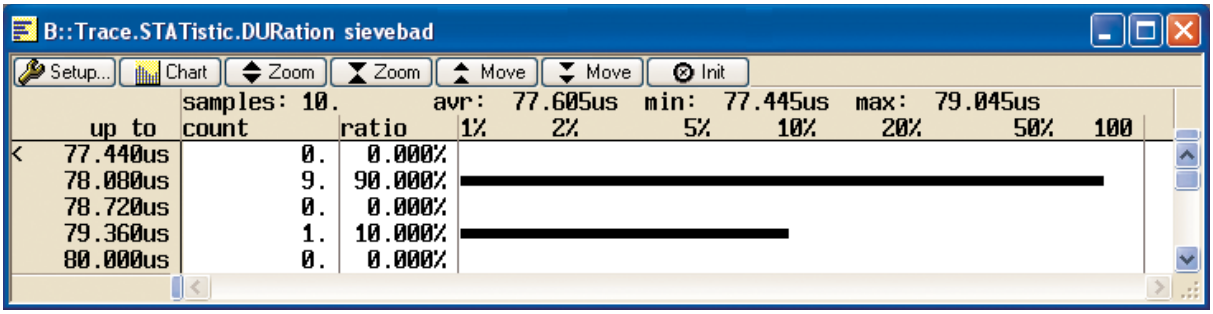

Figure 10: Run-time analysis of the sievebad function using TRACE32-PowerTrace

By redirecting the address of one of the competing program instructions to the end address 0x190, the competition is removed from cache line 0x15. As only two addresses are now competing for this cache line, there is no need for further eviction. An analysis of the optimized function (sievegood) shows an immediate and considerable improvement in run-time performance. The run time is on average only 7.9 us.

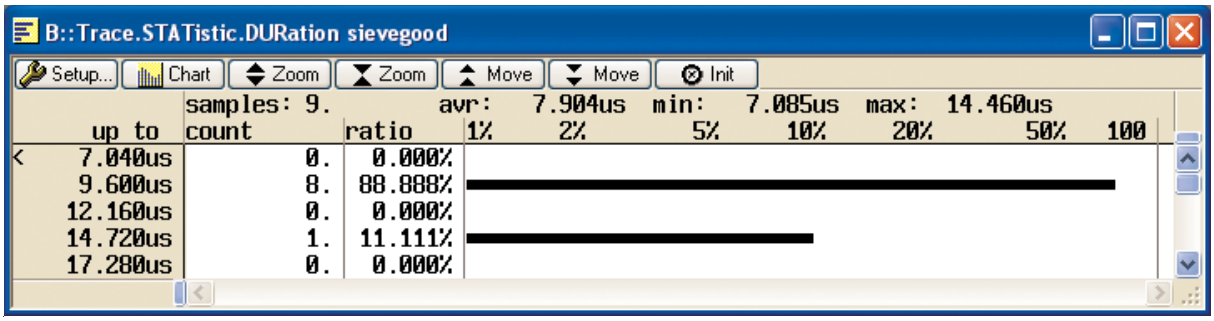

Figure 11: Run-time analysis of the sievegood function using TRACE32-PowerTrace

Using a combination of cache analysis and run-time measurements, developers can use TRACE32-PowerTrace to test whether optimized cache efficiency actually leads to the predicted improvement in run times. It can also be used to investigate if code optimizations impair cache efficiency and therefore do not improve program run times.

Summary

The latest cache analysis tool from Lauterbach Datentechnik GmbH provides developers of embedded systems with the following benefits:

- ❏ Optimization of program run times
- ❏ Reduction in power consumption of the entire system

Cache analysis can be performed on all microcontrollers, cache architectures, and cache hierarchies. If required, the predefined cache structure of microcontrollers can also be modified. In this way, an alternative cache structure can be tested to determine if its use will lead to greater cache efficiency and therefore shorten program run times. The result can then be taken into account for future designs.

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Disclaimer

The information presented is intended to give overview information only. Changes and technical enhancements or modifications can be made with-