

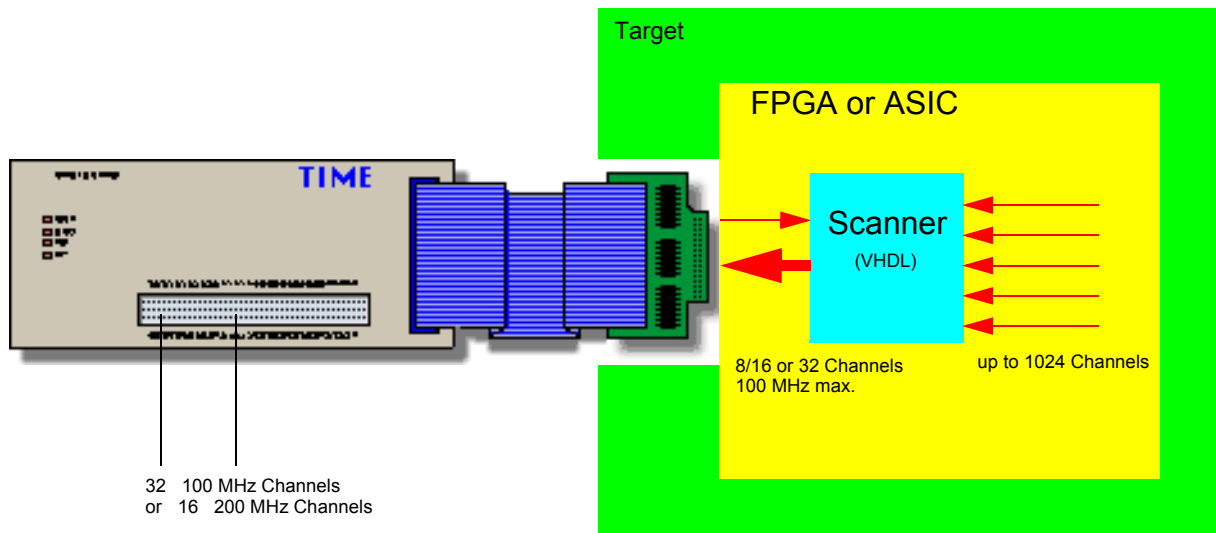
Adapter for SOC Trace

- Trace of up to 1024 Signals
- 100 MHz Sample Rate
- 32 Multiplexed Channels
- Scalable Trace Connector
- Easy Adaption

Function

The adapter for SOC Trace enables trace of internal signals in FPGA and ASIC devices. The trace data are sampled inside the chip and send-out on up to 32 multiplexed trace channels. The multiplexer is controlled by the logic analyzer. If all channels are inside one

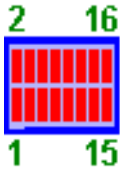
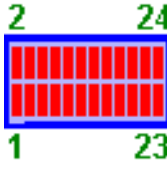
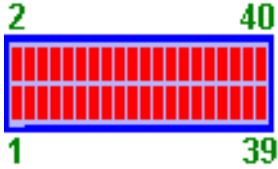
32 bit block, the logic analysis can run at 100 MHz. If signals out of two groups should be sampled at the same time, the sample rate is 50 MHz. Up to 1024 channels can be traced by the scanner module.



Connector Version A (0.8 mm SAMTEC)

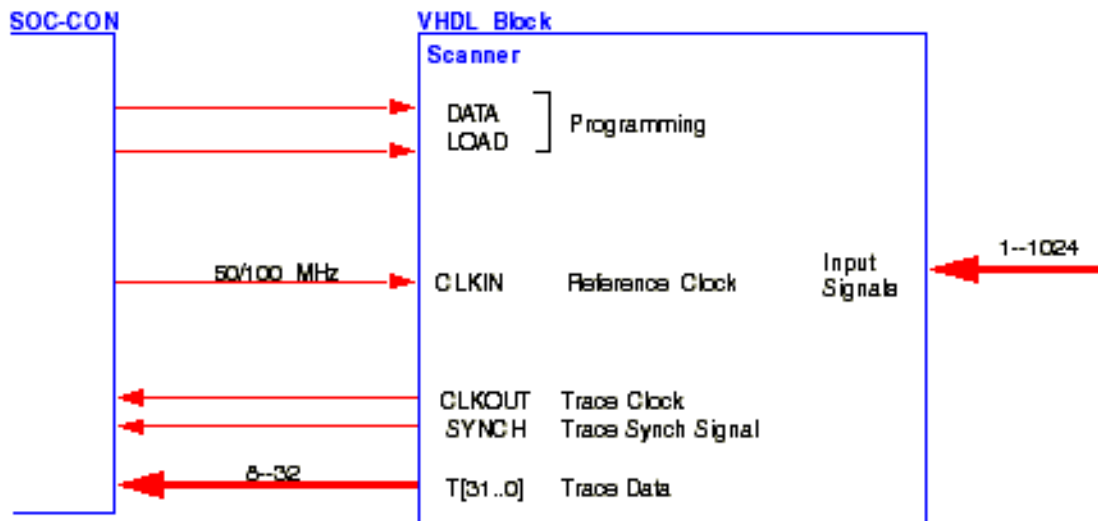
3 types of connectors are defined. The connector type is very small and can be placed also on production PCB.

Connector Type

Connector	Trace Channels
Samtec FTE-108-01-G 	8
Samtec FTE-112-01-G 	16
Samtec FTE-120-01-G 	32

Signals

Signal	Pin	Pin	Signal
GND	1	2	LOAD
DATA	3	4	CLKIN
CLKOUT	5	6	SYNCH
T00	7	8	T01
T02	9	10	T03
T04	11	12	T05
T06	13	14	T07
GND	15	16	VCC
T08	17	18	T09
T10	19	20	T11
T12	21	22	T13
T14	23	24	T15
T16	25	26	T17
T18	27	28	T19
T20	29	30	T21
T22	31	32	T23
T24	33	34	T25
T26	35	36	T27
T28	37	38	T29
T30	39	40	T31



Connector Version B (MICTOR)

Signals

Signal	Pin	Pin	Signal
VCC	1	2	LOAD-
CLKIN	3	4	DATA
CLKOUT	5	6	SYNCH
T15	7	8	T31
T14	9	10	T30
T13	11	12	T29
T12	13	14	T28
T11	15	16	T27
T10	17	18	T26
T09	19	20	T25
T08	21	22	T24
T07	23	24	T23
T06	25	26	T22
T05	27	28	T21
T04	29	30	T20
T03	31	32	T19
T02	33	34	T18
T01	35	36	T17
T00	37	38	T16

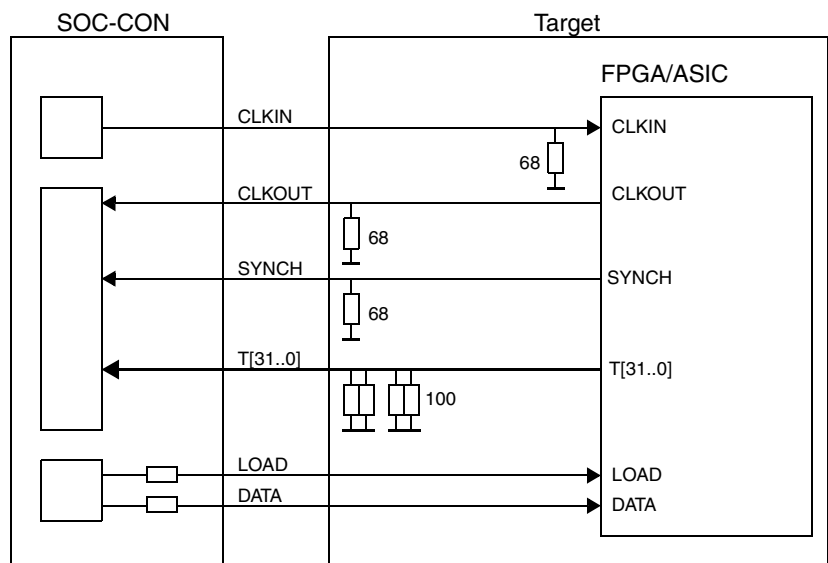
Pins 39 to 43 must be connected to GND

Scanner Module and Timing

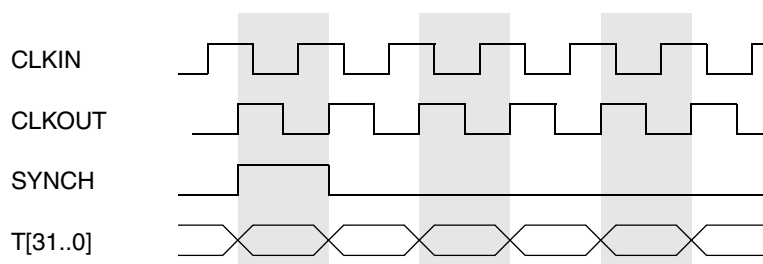
General

The scanner module has up to 1024 signal inputs for customer usage, 2 control lines for programming, one clock input for the scanner clock, one

reference clock output, a synchronisation signal and up to 32 multiplexed trace signals.



Timing



CLKIN

The scanner module runs at 100 MHz. The input clock is supplied by the trace

module. For slower designs the input clock can be reduced to 50 MHz. The input clock has 2.5 V high value and a driver impedance of 20 Ohm. The input clock should be terminated by a 68

Ohm resistor. For 1.8V systems the clock can be divided by an 22 and 47 Ohm resistor.

CLKOUT

All output signals are related to the CLKOUT signal. Output signals should switch at ± 2 ns related the rising edge of CLKOUT. CLKOUT should be terminated with 68 Ohm, if the line length on the target board is larger than 20 mm.

T[31..0]

The trace data are synchronous with the CLKOUT signal (± 2 ns). The threshold level is 1.4V (1.0V optional for 1.8V systems.) T[31..0] should be terminated by 100 Ohm, if the line length on the target board is larger than 40 mm.

SYNCH

SYNCH marks the start of the multiplexer sequence. Synch is synchronous with CLKOUT (± 2 ns). The threshold level is 1.4V (1.0V optional for 1.8V systems.)

LOAD

The LOAD input is uncritical, no termination is necessary.

DATA

The DATA input is uncritical, no termination is necessary.

Code

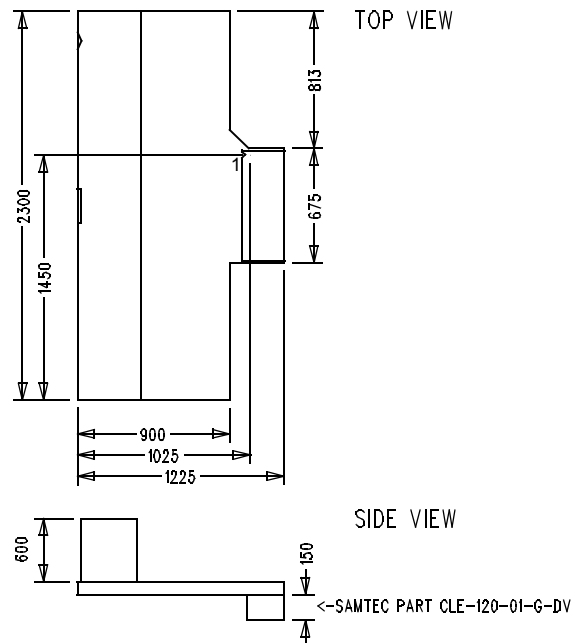
Please send a EMAIL to

support@lauterbach.com

for receiving the the code for the scanner block. The code is written in VHDL and AHDL (Altera),

Dimensions

Adapter Dimensions



Contact

International Representative

Argentina

Anacom Eletronica Ltda.
Mr. Rafael Sorice
Rua Nazareth, 807, Barcelona
BR-09551-200 São Caetano do Sul, SP
Phone: +55 11 3422 4200
FAX: +55 11 3422 4242
EMAIL: rsorice@anacom.com.br

Australia

Embedded Logic Solutions P/L
Mr. Ramzi Kaffan
Suite 2, Level 3
144 Marsden Street
Parramatta NSW 2150
Phone: +61 2 9687 1880
FAX: +61 2 9687 1881
EMAIL: sales@emlogic.com.au

Austria

Lauterbach GmbH
Altlaufstr. 40
D-85635 Höhenkirchen-Siegertsbrunn
Phone: +49 8102 9876 0
FAX: +49 8102 9876 999
EMAIL: info@lauterbach.com

Belgium

Tritec Benelux B.V.
Mr. Robbert de Voogt
Stationspark 550
NL-3364 DA Slidrecht
Phone: +31 184 41 41 31
FAX: +31 184 42 36 11
EMAIL: software@tritec.nl

Brazil

Anacom Eletronica Ltda.
Mr. Rafael Sorice
Rua Nazareth, 807, Barcelona
BR-09551-200 São Caetano do Sul, SP
Phone: +55 11 3422 4200
FAX: +55 11 3422 4242
EMAIL: rsorice@anacom.com.br

Canada

Lauterbach Inc.
Mr. Udo Zoettler
4 Mount Royal Ave.
USA-Marlborough, MA 01752
Phone: +1 508 303 6812
FAX: +1 508 303 6813
EMAIL: info_us@lauterbach.com

China Beijing

Lauterbach Technologies Co., Ltd
Mr. Linglin He
Beijing Office
A3, South Lishi Road, XiCheng District
Beijing 100037, P.R. China
Phone: +86 10 68023502
FAX: +86 10 68023523
EMAIL: linglin.he@lauterbach.com

China Shenzhen

Lauterbach Technologies Co., Ltd
1406/E Xihaimingzhu Building
No.1 Taoyuan Road, Nanshan District
Shenzhen 518052, P.R. China
Phone: +86 755 8621 0671
FAX: +86 755 8621 0675
EMAIL: emily.zhang@lauterbach.com

China Suzhou

Lauterbach Technologies Co., Ltd
Mr. Linglin He
Hengyu Square, Rm 709
No. 188, Xing Hai Street
Suzhou, 215021 P.R. of China
Phone: +86 512 6265 8030
FAX: +86 512 6265 8032
EMAIL: info_cn@lauterbach.com

Czech Republic

Lauterbach GmbH
Altlaufstr. 40
D-85635 Höhenkirchen-Siegertsbrunn
Phone: +49 8102 9876 0
FAX: +49 8102 9876 999
EMAIL: info@lauterbach.com

Denmark

Nohau Danmark A/S
Mr. Flemming Jensen
Klausdalsbrovej 493
DK-2730 Herlev
Phone: +45 44 52 16 50
FAX: +45 44 52 26 55
EMAIL: info@nohau.dk

Egypt

Wantech Egypt
Mr. Wagih A. Nawara
5 Shafik Ghalie St., Suite 2
Off Pyramids Road, Giza
Cairo 12111
Phone: +20 100 1251955
FAX: +20 100 1250349
EMAIL: sales@wantech.net.com

Finland

Nohau Solutions Finland
Mr. Martti Viljainen
Teknobulevardi 3-5
FI-01531 Vantaa
Phone: +358 40 546 1469
FAX: +358 9 2517 8101
EMAIL: sales@nohau.fi

France

Lauterbach S.A.R.L.
Mr. Jean-Pierre Paradiso
Europarc - Le Hameau B
135 Chemin Des Bassins
F-94035 Créteil Cedex
Phone: +33 1 49 56 20 30
FAX: +33 1 49 56 20 39
EMAIL: info_fr@lauterbach.com

Germany

Lauterbach GmbH
Altlaufstr. 40
D-85635 Höhenkirchen-Siegertsbrunn
Phone: +49 8102 9876 0
FAX: +49 8102 9876 999
EMAIL: info@lauterbach.com

Germany North

Lauterbach GmbH
Mr. Klaus Hommann
Leonhardring 5
D-31319 Sehnde
Phone: +49 8102 9876 174
FAX: +49 5138 6185 3
EMAIL: klaus.hommann@lauterbach.com

Germany South

Lauterbach GmbH
 Andreas Grimm
 Altlaufstr. 40
 D-85635 Höhenkirchen-Siegertsbrunn
 Phone: +49 8102 9876 190
 FAX: +49 8102 9876 187
 EMAIL: andreas.grimm@lauterbach.com

Greece

Lauterbach GmbH
 Altlaufstr. 40
 D-85635 Höhenkirchen-Siegertsbrunn
 Phone: +49 8102 9876 0
 FAX: +49 8102 9876 999
 EMAIL: info@lauterbach.com

Hungary

Lauterbach GmbH
 Altlaufstr. 40
 D-85635 Höhenkirchen-Siegertsbrunn
 Phone: +49 8102 9876 0
 FAX: +49 8102 9876 999
 EMAIL: info@lauterbach.com

India-Bangalore

Electro Systems Associates Pvt. Ltd.
 Mr. G. V. Gurunatham
 S-606, World Trade Center
 Malleswaram West, No.26/1, Dr. Rajkumar
 Road
 India - Bangalore 560055
 Phone: +91 80 67648888
 FAX: +91 80 23475615
 EMAIL: Trace32sales@esaindia.com

India-Chennai

Electro Systems Associates Pvt. Ltd.
 Mr. D. Kannan
 No.109/59A, Ground Floor
 IV Avenue, Ashok Nagar
 India - Chennai - 600 083 Tamilnadu
 Phone: +91 044-24715750
 FAX: +91 44 24715750
 EMAIL: chennai@esaindia.com

India-Delhi

Electro Systems Associates Pvt. Ltd.
 Mr. R.K. Bhandari
 No. 705, 7th Floor, Laxmi Deep
 Shivajinagar
 India - Delhi - 110 092
 Phone: +91 11-22549351
 FAX:
 EMAIL: delhi@esaindia.com

India-Hyderabad

Electro Systems Associates Pvt. Ltd.
 Mr. C.V.M. Sri Ram Murthy
 Shop No. 14, "Global Enclave"
 Bhagyannagar Colony, Kukat pally
 India - Hyderabad 500 072
 Phone: +91 40-23063346
 FAX: +91 40-23063346
 EMAIL: hyderabad@esaindia.com

India-Pune

Electro Systems Associates Pvt. Ltd.
 Mr. R K Bhandari
 Shriram Complex, 1126/1, Model Colony
 Shivajinagar
 India - Pune - 411 016
 Phone: +91 20 - 30462035 / 25663
 FAX: +91 20-25677202
 EMAIL: pune@esaindia.com

Ireland

Lauterbach Ltd.
 Mr. Barry Lock
 11 Basepoint Enterprise Centre
 Stroudley Road
 Basingstoke, Hants RG24 8UP
 Phone: +44-1256-333-690
 FAX: +44-1256-336-661
 EMAIL: info_uk@lauterbach.com

Israel

Itec Ltd.
 Mr. Mauri Gottlieb
 P.O. Box 10002
 IL-Tel Aviv 61100
 Phone: +972 3 6491202
 FAX: +972 3 6497661
 EMAIL: general@itec.co.il

Italy

Lauterbach Srl
 Mr. Maurizio Menegotto
 Via Enzo Ferrieri 12
 I-20153 Milano
 Phone: +39 02 45490282
 FAX: +39 02 45490428
 EMAIL: info_it@lauterbach.com

Japan

Lauterbach Japan, Ltd.
 Mr. Kenji Furukawa
 3-8-8 Shinyokohama
 Kouhoku-ku, Nisso 16th Building
 Yokohama-shi, Japan 222-0033
 Phone: +81 45 477 4511
 FAX: +81 45 477 4519
 EMAIL: info@lauterbach.co.jp

Luxembourg

Tritec Benelux B.V.
 Mr. Robbert de Voogt
 Stationspark 550
 NL-3364 DA Sliedrecht
 Phone: +31 184 41 41 31
 FAX: +31 184 42 36 11
 EMAIL: software@tritec.nl

Malaysia

Flash Technology
 Mr. Teo Kian Hock
 No 61, # 04-15 Kaki Bukit Av 1
 Shun Li Industrial Park
 SGP-Singapore 417943
 Phone: +65 6749 6168
 FAX: +65 6749 6138
 EMAIL: teokh@flashtech.com.sg

Mexico

Lauterbach Inc.
 Mr. Udo Zoettler
 4 Mount Royal Ave.
 USA-Marlborough, MA 01752
 Phone: +1 508 303 6812
 FAX: +1 508 303 6813
 EMAIL: info_us@lauterbach.com

Netherlands

Tritec Benelux B.V.
 Mr. Robbert de Voogt
 Stationspark 550
 NL-3364 DA Sliedrecht
 Phone: +31 184 41 41 31
 FAX: +31 184 42 36 11
 EMAIL: software@tritec.nl

New Zealand

Embedded Logic Solutions P/L
 Mr. Ramzi Kattan
 Suite 2, Level 3
 144 Marsden Street
 Parramatta NSW 2150
 Phone: +61 2 9687 1880
 FAX: +61 2 9687 1881
 EMAIL: sales@emlogic.com.au

Norway

Nohau Solutions AB
 Mr. Jörgen Nilsson
 Derbyvägen 4
 SE-21235 Malmö
 Phone: +46 40 592 206
 FAX: +46 40 592 229
 EMAIL: sales@nohau.se

Poland

QUANTUM Sp. z o.o.
 Mr. Aleksander Bil
 ul. Jeleniogorska 6
 54-056 Wrocław
 Phone: +48 71 362 6356
 FAX: +48 71 362 6357
 EMAIL: info@quantum.com.pl

Portugal

Captura Electronica, SCCL
Mr. Juan Martinez
c/Duero, 40
E-08031 Barcelona
Phone: +34 93 429 5730
FAX: +34 93 407 0778
EMAIL: info@captura-el.com

Romania

Lauterbach GmbH
Altlaufstr. 40
D-85635 Höhenkirchen-Siegersbrunn
Phone: +49 8102 9876 0
FAX: +49 8102 9876 999
EMAIL: info@lauterbach.com

Russia

RTSoft
Mr. Alexey Isaev
Nikitinskaya 3
RUS-105037 Moscow
Phone: +7 495 742 6828
FAX: +7 495 742 6829
EMAIL: sales@rtsoft.msk.ru

Singapore

Flash Technology
Mr. Teo Kian Hock
No 61, # 04-15 Kaki Bukit Av 1
Shun Li Industrial Park
SGP-Singapore 417943
Phone: +65 6749 6168
FAX: +65 6749 6138
EMAIL: teokh@flashtech.com.sg

South Korea, Pangyo

MDS Technology Co., Ltd.
Mr. Sangheon Lee
3FL, Hancom Tower
49, Daewangpangyo-ro 644, Bundang-gu
Seongnam-si, Gyeonggi-do, 463-400, ROK
Phone: +82-31-627-3000
FAX: +82-31-627-3100
EMAIL: trace32@mdstec.com

Spain

Captura Electronica, SCCL
Mr. Juan Martinez
c/Duero, 40
E-08031 Barcelona
Phone: +34 93 429 5730
FAX: +34 93 407 0778
EMAIL: info@captura-el.com

Sweden

Nohau Solutions AB
Mr. Jörgen Nilsson
Derbyvägen 4
SE-21235 Malmö
Phone: +46 40 592 206
FAX: +46 40 592 229
EMAIL: sales@nohau.se

Switzerland

JDT Jberg DatenTechnik
Mr. Andreas Jberg
Zimmereistrasse 2
CH-5734 Reinach AG
Phone: +41 62 7710 886
FAX:
EMAIL: Andreas.Jberg@jdt.ch

Taiwan

Superlink Technology Corp.
Mr. Sulin Huang
3F-8, No. 77, Sec. 1, Xintaiwu Rd., Xizhi District,
New Taipei City 22101, Taiwan, R.O.C.
Phone: +886 2 26983456
FAX: +886 2 26983535
EMAIL: info.stc@superlink.com.tw

Tunisia

Lauterbach Consulting S.A.R.L.
Mr. Khaled Jmal
Route El Ain Km 3.5
TN-3062 Sfax
Phone: +216-74611730
FAX: +216-74611723
EMAIL: info_tn@lauterbach.com

Turkey-1

Tektronik Muh. ve Tic. A.S.
Mr. Hakan Yavuz
CyberPlaza B-Blok, 702B
Bilkent
06800 Ankara
Phone: +90 312 437 3000
FAX: +90 312 437 1616
EMAIL: info@tektronik.com.tr

Turkey-2

G3TEK Embedded Technologies Ltd.
Mr. Celal Aygun
Ilkyerlesim Mah. 445.
Sok. No: 48
06370 Batikent/Ankara
Phone: +90 312 3324769
FAX: +90 312 3324769
EMAIL: info@g3tek.com

UK

Lauterbach Ltd.
Mr. Barry Lock
11 Basepoint Enterprise Centre
Stroudley Rd
Basingstoke, Hants RG24 8UP
Phone: +44 1256 333 690
FAX: +44 1256 350 301
EMAIL: info_uk@lauterbach.com

USA East

Lauterbach Inc.
Mr. Udo Zoettler
4 Mount Royal Ave.
USA-Marlborough, MA 01752
Phone: +1 508 303 6812
FAX: +1 508 303 6813
EMAIL: info_us@lauterbach.com

USA West

Lauterbach Inc.
Mr. Bob Kupyn
1111 Main Street, Suite 620
USA-Vancouver, WA, 98660
Phone: +1 503 524 2222
FAX: +1 503 524 2223
EMAIL: bob.kupyn@lauterbach.com

Additional Information

<http://www.lauterbach.com>

Lauterbach GmbH

Altlaufstr. 40
D-85635 Höhenkirchen-Siegertsbrunn
Tel. ++49 8102 9876-0 FAX -999
info@lauterbach.com
http://www.lauterbach.de

Lauterbach Inc.

4 Mount Royal Ave.
Marlboro MA 01752
Phone (508) 303 6812 FAX (508) 303 6813
info_us@lauterbach.com
http://www.us.lauterbach.com

Lauterbach Ltd.

11 Basepoint Enterprise Ctre Stroudley Road
Basingstoke, Hants RG24 8UP
Phone ++44-1256-333-690 FAX -661
info_uk@lauterbach.com
http://www.lauterbach.co.uk

Lauterbach S.A.R.L.

135 Chemin Des Bassins
F-94035 Créteil Cedex
Phone ++33-149-562-030
FAX ++33-149-562-039
info_fr@lauterbach.com
http://www.lauterbach.fr

Lauterbach Japan, Ltd.

3-9-5 Shinyokohama Kouhoku-ku
Yokohama-shi Japan 222-0033
Phone ++81-45-477-4511 FAX -4519
info_j@lauterbach.com
http://www.lauterbach.co.jp

Lauterbach s.r.l.

Lauterbach s.r.l.
Via Enzo Ferrieri 12
I-20153 Milano
Phone ++39 02 45490282
FAX ++39 02 45490428
info_it@lauterbach.it
http://www.lauterbach.it

Suzhou Lauterbach Consulting Co.,Ltd.

Room 1605, Xing Hai International Square
No.200, Xing Hai Street
Suzhou, 215021 PR of China
Phone: 0086-512 6265 8030
FAX: 0086-512 6265 8032
info_cn@lauterbach.cn
http://www.lauterbach.cn

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